Dual-Channel, High-Speed, Low-Side Gate Driver

GENERAL DESCRIPTION

The SLM27526 family of devices are dual-channel, high-speed, low-side gate drivers that can effectively drive MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, SLM27526 can source and sink high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay, typically 18 ns.

The SLM27526 provides 4.5 A source, 5.5 A sink peak drive current capability at 12V VDD supply.

APPLICATIONS

- Switching mode power supplies
- DC-to-DC converters
- Motor Control, solar power
- Gate driver for emerging wide band-gap power devices such as GaN

FEATURES

- Two independent gate drive channels
- 4.5 A peak source and 5.5 A peak sink current drive capability
- Fast propagation delay (18 ns typical)
- Fast rise and fall time (7 ns and 6 ns typical)
- 4.5 to 20V single supply range
- Under-voltage lockout
- TTL and CMOS compatible input logic threshold
- Ability to handle negative voltages (-5V) at inputs
- 2 ns typical delay matching between 2 channels
- Two outputs are paralleled for higher drive current
- Outputs held in low when inputs floating
- Operating temperature range of -40°C to 140°C
- DFN3x3-8 package

TYPICAL APPLICATION CIRCUIT

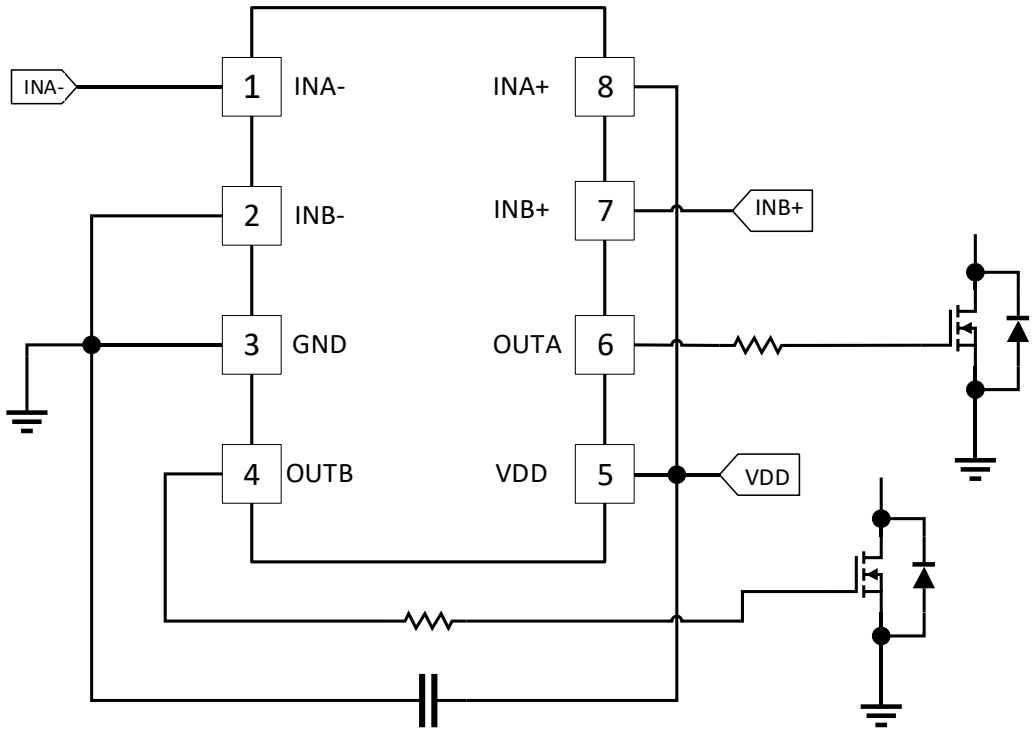

Figure 1. Typical Application Circuit

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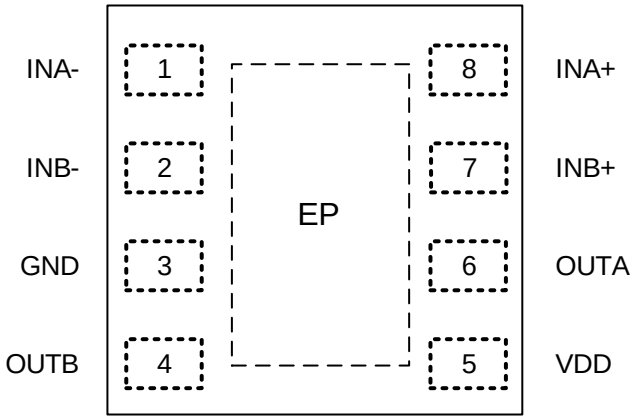
PIN CONFIGURATION

Package	SLM27526(Top View)
DFN3x3-8	

PIN DESCRIPTION

No.	Pin	Description
1	INA-	Inverting Input to Channel A: When Channel A is used in Non-Inverting configuration, connect INA– to GND in order to Enable Channel A output, OUTA held LOW if INA– is unbiased or floating
2	INB-	Inverting Input to Channel B: When Channel B is used in Non-Inverting configuration, connect INB– to GND in order to Enable Channel B output, OUTB held LOW if INB– is unbiased or floating.
3	GND	Ground: All signals are referenced to this pin.
4	OUTB	Output of channel B.
5	VDD	Bias Supply Input.
6	OUTA	Output of channel A
7	INB+	Non-Inverting Input to Channel B: When Channel B is used in Inverting configuration, connect INB+ to VDD in order to Enable Channel B output, OUTB held LOW if INB+ is unbiased or floating
8	INA+	Non-Inverting Input to Channel A: When Channel A is used in Inverting configuration, connect INA+ to VDD in order to Enable Channel A output, OUTA held LOW if INA+ is unbiased or floating
	EP	Exposed pad, connect to ground.

FUNCTIONAL BLOCK DIAGRAM

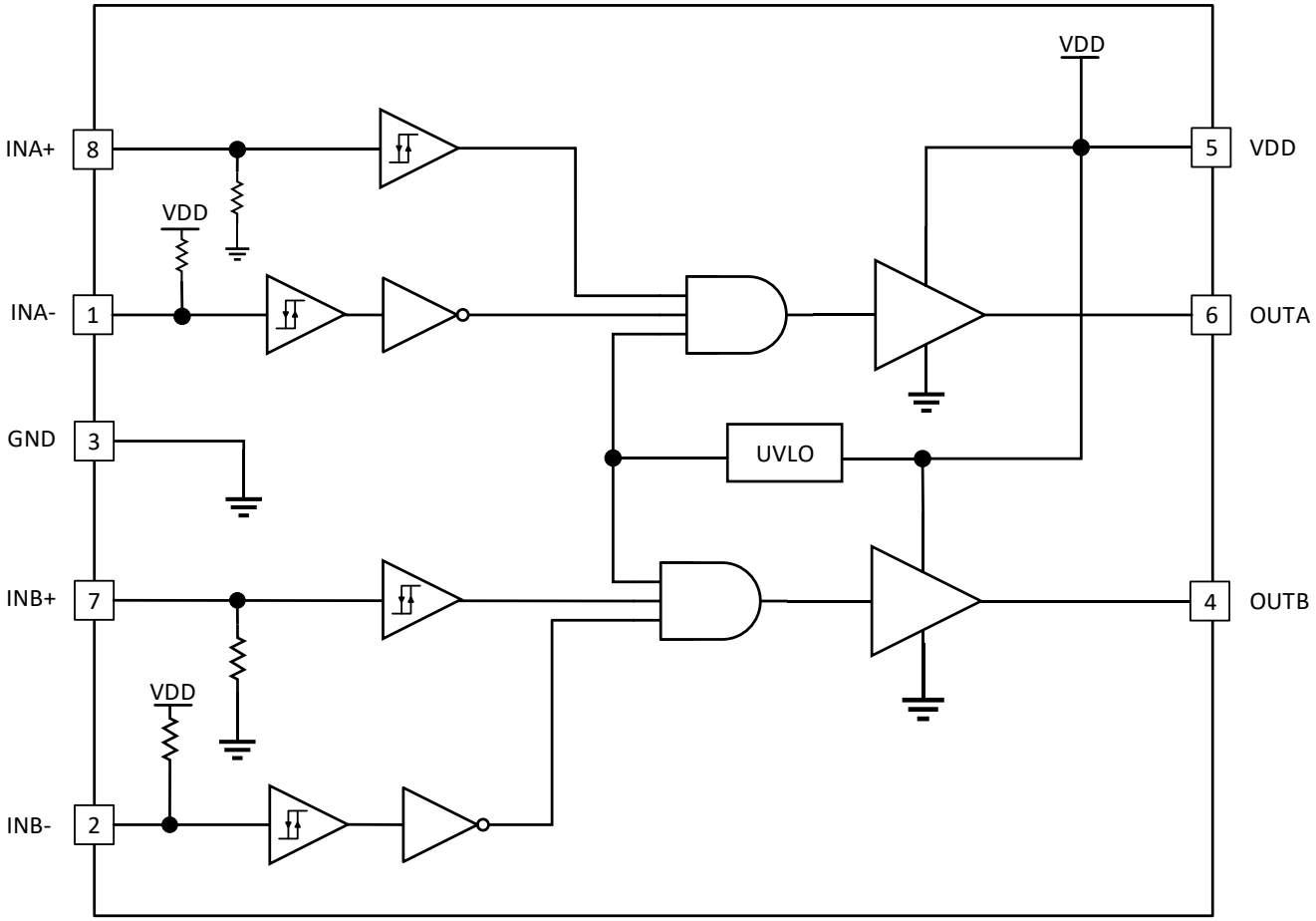


Figure 2. SLM27526 Block Diagram

ABSOLUTE MAXIMUM RATINGS[1,2,3]

Symbol	Description	Min.	Max.	Units
V_{DD}	Supply voltage	-0.3	25	V
V_O	Continuous voltage on OUTx	-0.3	V_{DD}+0.3	
	Repetitive pulse less than 200ns[4]	-2	V_{DD}+0.3	
I_O	Source Continuous Current on OUTx		0.3	A
	Source Pulsed Current on OUTx (0.5 μs) [4]		4.5	
	Sink Pulsed Current on OUTx (0.5 μs) [4]		5.5	
INA+, INA-, INB+, INB-	Voltage on INA+, INA-, INB+,INB-.	-6	25	V
T_J	Operation junction temperature range	-40	150	°C
T_L	Lead temperature (soldering, 10 seconds)		300	
T_S	Storage temperature	-55	150	

1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2) All voltages are with respect to GND unless otherwise noted.

3) These devices are sensitive to electrostatic discharge; follow proper device-handling procedures.

4) Values are verified by characterization on bench.

RECOMMENDED OPERATION CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Definition	Min	Max	Units
V_{DD}	Supply voltage	4.5	20	V
INA+, INA-, INB+, INB-	Input voltage	-5	20	
T_J	Operation junction temperature range	-40	140	°C

ORDERING INFORMATION

Order Part No.	Package	QTY
SLM27526EN-DG	DFN3x3-8, Pb-Free	3000/Reel

DYNAMIC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Rise time[1]	C_L = 1.8 nF		7	15	ns
t_F	Fall time[1]	C_L = 1.8 nF		6	10	
t_M	Delay matching between two channels	INA+ = INB+, INA-= INB-,OUTA and OUTB at 50% transition point		2	4	
t_{PW}	Minimum input pulse width that changes the output state[2]			15	25	
t_{D1}, t_{D2}	Input to output propagation delay[1]	C_L = 1.8 nF, 5 V input pulse	7	18	26	

1) See timing diagrams in Figure 3 and Figure 4

2) Values are verified by characterization on bench.

STATIC ELECTRICAL CHARACTERISTICS

V_{DD}= 12 V, C_L = 1000 pF and T_J = -40°C to 140°C unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD(off)}$	Startup current	V_{DD} = 3.4 V INA+ = INB+ = V_{DD} INA- = INB- = GND	55	110	250	uA
		VDD = 3.4 V, INA+ = INB+=GND INA-= INB-= GND	55	110	250	
V_{DDUV+}	Undervoltage positive going threshold	T_J = 25 °C	3.9	4.2	4.5	V
		T_J = –40 °C to 140 °C	3.8	4.2	4.6	
V_{DDUV-}	Undervoltage negative going threshold		3.7	3.9	4.4	
V_{DD_H}	Supply voltage hysteresis			0.3		
V_{IH}	Input signal high threshold	Applied to INA+, INA-, INB+, INB-	1.6	1.9	2.3	V
V_{IL}	Input signal low threshold	Applied to INA+, INA-, INB+ INB-	1.0	1.3	1.5	
I_O	Source peak current	C_L = 0.22 µF		4.5		A
	Sink peak current	C_L = 0.22 µF		5.5		
V_{OH}	High level output voltage	I_O = –10 mA, V_{DD}-V_O		0.008	0.016	V
V_{OL}	Low output voltage	I_O = 10 mA		0.005	0.009	
R_{OH}	Output pull-up resistance	I_O = –10 mA	0.5	0.8	1.6	Ω
R_{OL}	Output pull-down resistance	I_O = 10 mA	0.3	0.5	0.9	

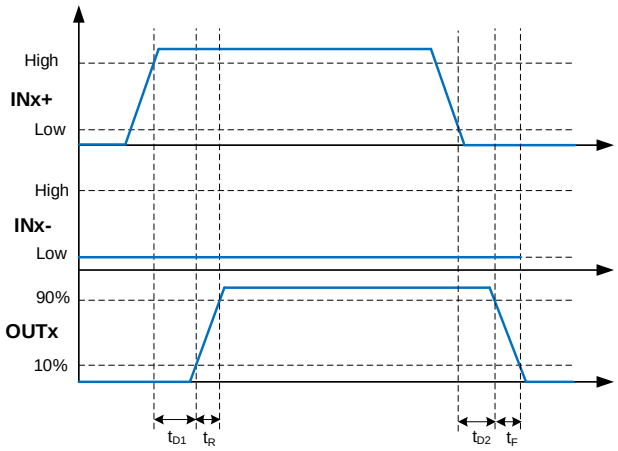


Figure 3. Non-Inverting Input Driver Operation

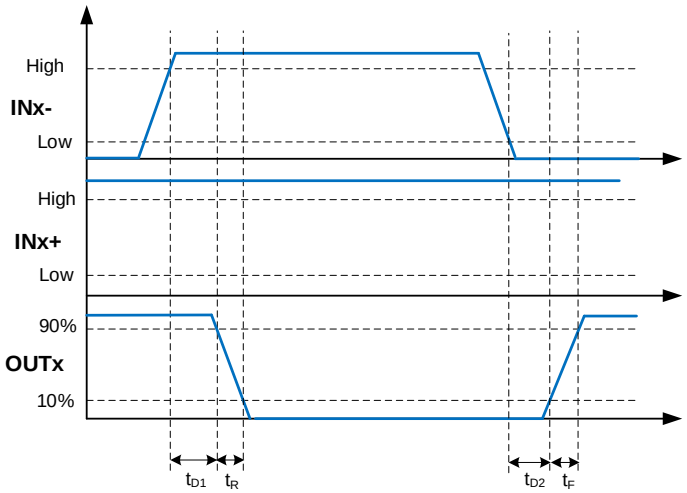


Figure 4. Inverting Input Driver Operation

FEATURE DESCRIPTION

VDD and Under-Voltage Lockout

The SLM27526 device has internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (for example when V_{DD} voltage is less than V_{DDUV+} during power up or when VDD voltage is less than V_{DDUV-} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} supply voltage have noise from the power supply and also when there are droops in the VDD bias voltage when the system starts switching and there is a sudden increase in I_{DD}.

Input Stage

The input pins of the SLM27526 gate driver are based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With typically high threshold = 1.9 V and typically low threshold = 1.3 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3V and 5V digital power-controller devices. SLM27526 also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The SLM27526 features an important safety feature wherein, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using GND pull-down resistors on all the non-inverting input pins (INA+, INB+) and V_{DD} pull-up resistors on all the inverting input pins (INA-, INB-), as shown in the device block diagrams.

The SLM27526 features a dual input configuration with two input pins available to control the output state of each channel. With the SLM27526 device the user has the flexibility to drive each channel using either a non-inverting input pin (INx+) or an inverting input pin (INx–). The state of the output pin is dependent on the bias on both the INx+ and INx– pins (where x = A, B). Once an Input pin is chosen to drive a channel, the other input pin of that channel (the unused input pin) must be properly biased in order to enable the output of the channel. The unused input pin cannot remain in a floating condition because, as mentioned earlier, whenever any input pin is left in a floating condition, the output of that channel is disabled using the internal pullup or pulldown resistors for safety purposes. Alternatively, the unused input pin is used effectively to implement an enable/disable function, as explained below.

• In order to drive the channel x (x = A or B) in a non-inverting configuration, apply the PWM control input signal to INx+ pin. In this case, the unused input pin, INx-, must be biased low (for example, tied to GND) in order to enable the output of this channel.

– Alternately, the INx– pin can be used to implement the enable/disable function using an external logic signal. OUTx is disabled when INx- is biased High and OUTx is enabled when INX– is biased low.

• In order to drive the channel x (x = A or B) in an Inverting configuration, apply the PWM control input signal to INX– pin. In this case, the unused input pin, INX+, must be biased high (for example, tied to VDD) in order to enable the output of the channel.

– Alternately, the INX+ pin can be used to implement the enable/disable function using an external logic signal. OUTX is disabled when INX+ is biased low and OUTX is enabled when INX+ is biased high.

• Finally, it is worth noting that the SLM27526 output pin can be driven into high state only when INx+ pin is biased high and INx- input is biased low.

Enable Function

The SLM27526 device does not feature dedicated enable pins. However, as mentioned earlier, an enable/disable function is easily implemented in SLM27526 using the unused input pin. When INx+ is pulled down to GND or INx– is pulled down to VDD, the output is disabled. Thus INx+ pin is used like an enable pin that is based on active high logic, while INx– is used like an enable pin that is based on active low logic. Note that the INx+, INx– pins in SLM27526 are not allowed to be floating because this will disable the outputs.

Output Stage

Each output stage in the SLM27526 device is capable of supplying 4.5 A peak source and 5.5 A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out.

The channel A and channel B outputs can be paralleled to provide higher driver current capability. In such application, the INA and INB need to be connected together and ENA, ENB also need be connected together.

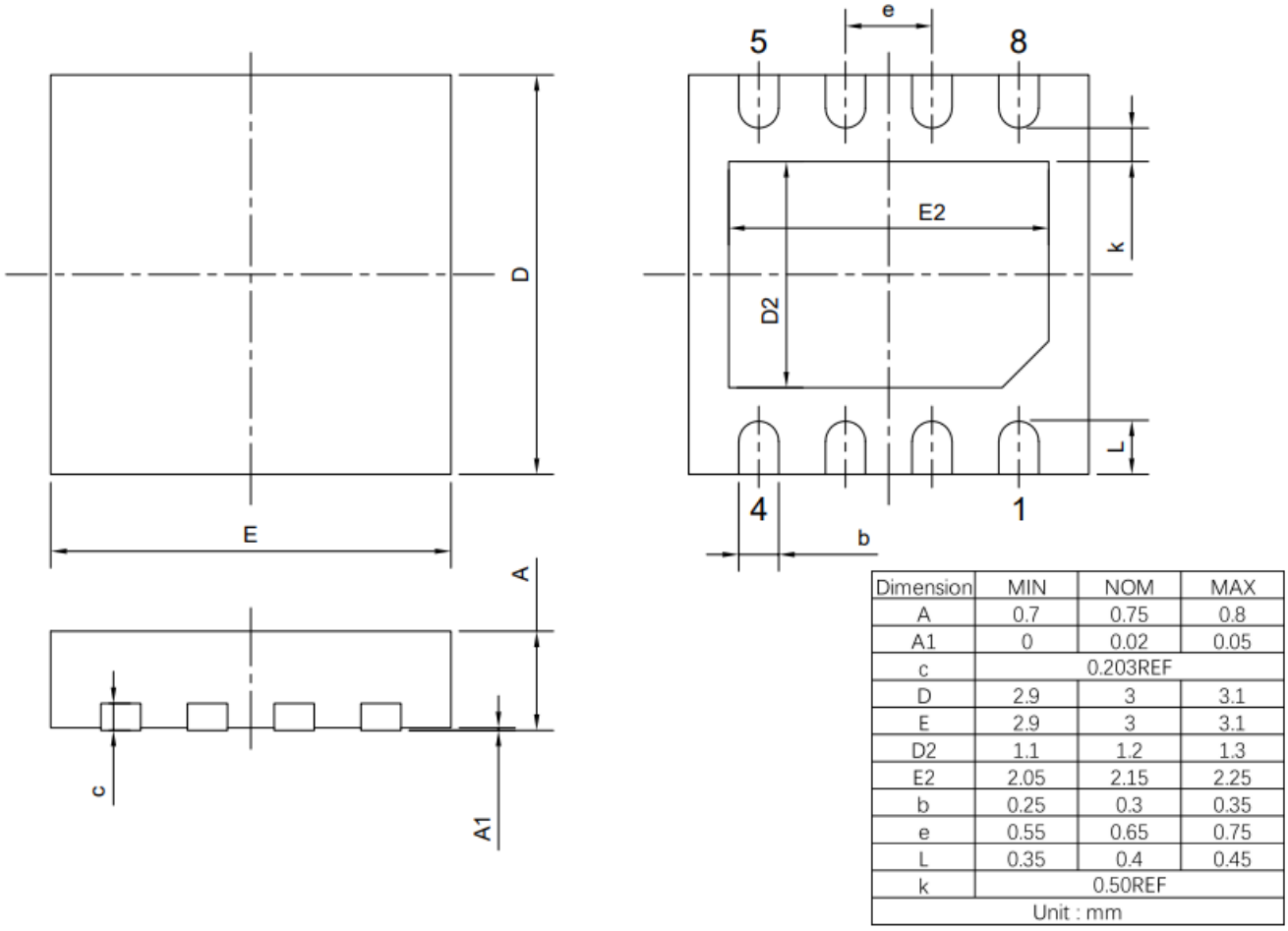
For example, in applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

Device Function Modes

Inx+ (x=A or B)	Inx- (x=A or B)	OUTx (x=A or B)
L	L	L
L	H	L
H	L	H
H	H	L
x(1)	Any	L
Any	x(1)	L

(1) x=floating condition

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
c		0.203REF	
D	2.9	3	3.1
E	2.9	3	3.1
D2	1.1	1.2	1.3
E2	2.05	2.15	2.25
b	0.25	0.3	0.35
e	0.55	0.65	0.75
L	0.35	0.4	0.45
k		0.50REF	
Unit : mm			

Figure 5. Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 **datasheet: 2022-05-09**	
Whole document	Initial release