

High CMTI, 12A Sink and Source Reinforced Isolated Single Channel Gate Driver with Split Output and Active Protection Features

GENERAL DESCRIPTION

The SiLM5992SH-AQ is an advanced single channel isolated gate driver with active protection features, such as desaturation detection, UVLO, isolated fault sensing and active miller clamp. Its peak output current is 12A for both source and sink.

The input side supply operates from 3V to 5.5V and the output side supply allows for a range from 13V to 30V. All the supply voltage pins have under voltage lock-out (UVLO) protection.

An internal desaturation (DESAT) fault detection recognizes when the IGBT is in an overcurrent condition. When desaturation is active, a fault signal is sent across the isolation barrier, pulling the $\overline{\text{FAULT}}$ output low at the input side and blocking the isolator input. When the IGBT is turned off during normal operation with bipolar output supply, the output is clamped to VEE2. If the output supply is unipolar, an active Miller clamp can be used, allowing Miller current to sink across a low impedance path, preventing IGBT to be dynamically turned on during high voltage transient conditions. The input side is isolated from output driver by a 5kV_{RMS} reinforced isolation barrier, with a minimum of 150kV/us common-mode transient immunity (CMTI).

APPLICATION

- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial power supplies

FEATURES

- AEC-Q100 qualified for automotive application
 - Temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- 12A source/sink output current with split output
- 4A active Miller clamping
- 550mA soft turn-off during short circuit
- Desaturation detection
- $\overline{\text{Fault}}$ alarm upon desaturation and reset from $\overline{\text{RST}}$
- VCC1 and VCC2 UVLO with RDY pin indication
- Active output pulldown and default low output with low supply or floating inputs
- CMOS compatible inputs
- Reject input pulses and noise transients shorter than 30ns
- 90ns (Typ) propagation delay
- 150kV/us (Min) common mode transient immunity (CMTI)
- Input side supply range from 3V to 5.5V
- Output side supply range from 13 V to 30 V
- SOP16W package with >8.0mm creepage and clearance
- Operating junction temperature: -40°C to $+150^{\circ}\text{C}$
- Safety certifications
 - 5kV_{RMS} isolation for 1 minute per UL 1577
 - CQC certification per GB4943.1-2022
 - DIN VDE 0884-17: 2021-10 (Pending)

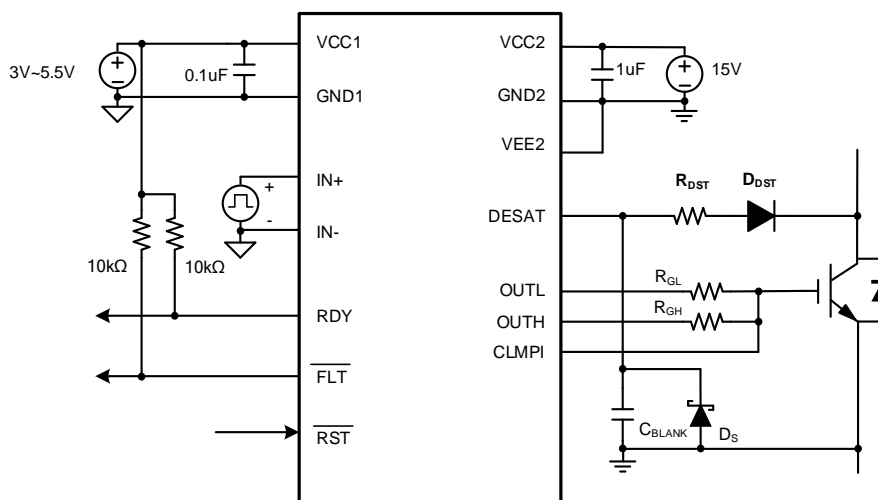
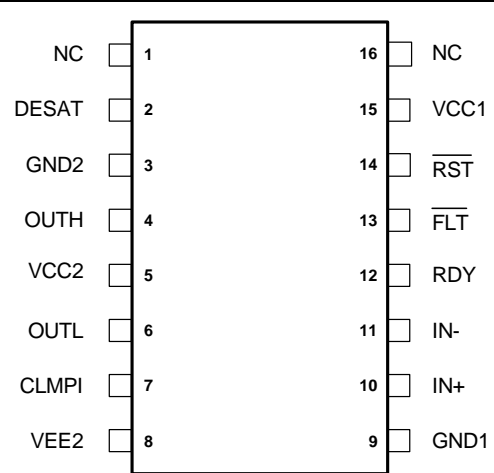


Figure 1. SiLM5992SH-AQ Application Circuit to Driver IGBT

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PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---------|--|
| SOP16W |  |

PIN DESCRIPTION

| No. | Pin | Description |
|-----|-------|--|
| 1 | NC | Not connected |
| 2 | DESAT | Desaturation current protection input. If not used, short to GND2 |
| 3 | GND2 | Common ground reference, connecting to emitter pin of IGBT or source pin of SiC/MOSFET |
| 4 | OUTH | Driver output pull up |
| 5 | VCC2 | Positive supply rail for driver voltage |
| 6 | OUTL | Driver output pull down |
| 7 | CLMPI | Internal active miller clamp. If not used, short to VEE2 |
| 8 | VEE2 | Negative supply rail for driver voltage |
| 9 | GND1 | Input power supply and logic ground reference |
| 10 | IN+ | Non-inverting driver control input |
| 11 | IN- | Inverting driver control input. If not used, short to GND1 |
| 12 | RDY | Power good for input and output side power supply. It is open drain configuration and can be paralleled with other RDY signals |
| 13 | FLT | Active low fault output upon over current detection. It is open drain configuration and can be paralleled with other fault signals |
| 14 | RST | Reset input, apply low pulse to reset fault latch |
| 15 | VCC1 | Input power supply |
| 16 | NC | Not connected |

FUNCTIONAL BLOCK DIAGRAM

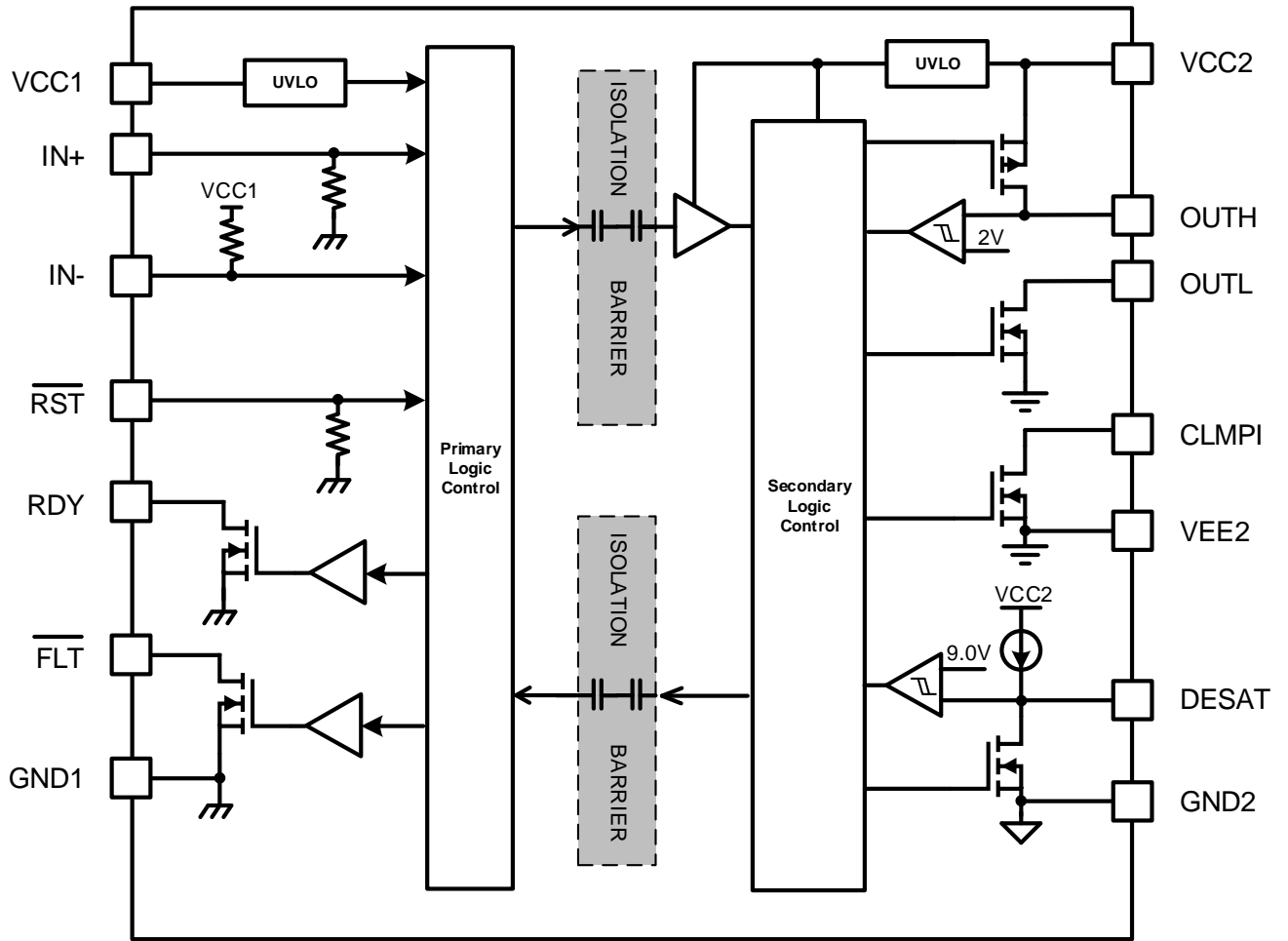


Figure 2. SiLM5992SH-AQ Block Diagram

ORDERING INFORMATION

| Order Part No. | Package | QTY |
|-----------------|-----------------|-----------|
| SiLM5992SHCG-AQ | SOP16W, Pb-Free | 1500/Reel |

ABSOLUTE MAXIMUM RATINGS

| Symbol | Definition | Min | Max | Units |
|-------------------|---|----------|--------------------------|-------|
| VCC1 -GND1 | Input Side Supply Voltage | -0.3 | 6 | V |
| VCC2 -VEE2 | Output Side Supply Voltage | -0.3 | 33 | V |
| VEE2 -GND2 | Negative Output Supply Voltage | -20 | 0.3 | V |
| VCC2 -GND2 | Positive Output Supply Voltage | -0.3 | 33 | V |
| DESAT | refer to GND2 | GND2-0.3 | Min(GND2 + 20, VCC2+0.3) | V |
| OUTH, OUTL, CLMPI | | VEE2-0.3 | VCC2+0.3 | V |
| RDY, FLT | | GND1-0.3 | VCC1 | V |
| IN+, IN-, RST | | GND1-2 | VCC1 | V |
| IFLT, IRDY | Output current of $\overline{\text{FLT}}$, RDY | | 20 | mA |
| T _J | Junction Temperature | -55 | 150 | °C |
| T _s | Storage Temperature | -65 | 150 | |

RECOMMENDED OPERATION CONDITIONS

| Symbol | Definition | Min | Max | Units |
|----------------|--------------------------------|-----|-----|-------|
| VCC1 -GND1 | Input Side Supply Voltage | 3 | 5.5 | V |
| VCC2 -VEE2 | Output Side Supply Voltage | 13 | 30 | V |
| VEE2 -GND2 | Negative Output Supply Voltage | -15 | 0 | V |
| VCC2 -GND2 | Positive Output Supply Voltage | 13 | 30 | V |
| T _J | Junction Temperature | -40 | 150 | °C |
| T _A | Ambient Temperature | -40 | 125 | °C |

ESD RATINGS

| Symbol | Definition | Value | Units |
|------------------|------------|-------|-------|
| V _{ESD} | HBM | ±8000 | V |
| | CDM | ±2000 | |

THERMAL INFORMATION¹

| Symbol | Definition | Value | Unit |
|-----------------------|---|-------|------|
| R _{θJA} | Junction to ambient thermal resistance | 100 | °C/W |
| R _{θJC(TOP)} | Junction to case (top) thermal resistance | 40 | °C/W |

Note1: Standard JESD51-3 low effective thermal conductivity test board.

PACKAGE SPECIFICATIONS

| Symbol | Definition | Min | Typ | Max | Units |
|-----------------|---|-----|------------------|-----|-------|
| R _{IO} | Resistance (Input Side to Output Side) | | 10 ¹² | | Ω |
| C _{IO} | Capacitance (Input Side to Output Side) | | 0.8 | | pF |

INSULATION SPECIFICATIONS

| Symbol | Definition | Test Condition | Value | Units |
|--|---|--|-----------|------------------|
| CLR | External clearance | Shortest terminal to terminal distance through air | 8.0 | mm |
| CPG | External creepage | Shortest terminal to terminal distance across the package surface | 8.0 | mm |
| DTI | Distance through the insulation | Minimum internal gap | >18 | um |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11), IEC 60112 | >600 | V |
| | Material Group | | I | |
| | Overvoltage category | Rated mains voltages ≤600Vrms | I-III | |
| | | Rated mains voltages ≤1000Vrms | I-II | |
| DIN V VDE 0884-11⁽¹⁾ | | | | |
| V _{IORM} | Maximum repetitive peak isolation voltage | | 1500 | V _{PK} |
| V _{IOWM} | Maximum isolation working voltage | AC voltage (sine wave) | 1060 | V _{RMS} |
| | | DC voltage | 1500 | V _{DC} |
| V _{IOTM} | Maximum transient isolation voltage | 60s | 7000 | V _{PK} |
| V _{IOSM} | Maximum surge isolation voltage | Test method per IEC62368, 1.2/50us waveform, V _{TEST} =1.6 x V _{IOSM} | 6250 | V _{PK} |
| q _{pd} | Apparent charge | Method b2: V _{pd(m)} =1.875 x V _{IORM} , t _m =1 s | ≤5 | pC |
| | Climatic Category | | 40/125/21 | |
| | Pollution Degree | | 2 | |
| UL1577 | | | | |
| V _{ISO} | Withstand Isolation Voltage | V _{TEST} =V _{ISO} , t=60s (qualification), V _{TEST} =1.2 x V _{ISO} , t=1s (100% production) | 5000 | V _{RMS} |

Note1: Certification pending

SAFETY RELATED CERTIFICATIONS

| VDE | UL | CQC |
|--------------------------|--|---|
| DIN VDE 0884-17: 2021-10 | UL 1577 component recognition program | Certified according to GB4943.1-2022 |
| Reinforced Insulation | Single protection, 5000 V _{RMS} | Reinforced insulation, Altitude ≤ 5000m |
| Pending | File number: E521801 | File number: CQC23001379622 |

SAFETY LIMITING VALUES

| Symbol | Parameter | Condition | Value | Unit | |
|----------------|---|---|-------------|------|----|
| I _s | Safety input, output, or supply current | R _{θJA} =100°C/W, V _{CC2} -V _{EE} = 15V, T _J =150°C, T _A =25°C | 80 | mA | |
| | | R _{θJA} =100°C/W, V _{CC2} -V _{EE} = 30V, T _J =150°C, T _A =25°C | 40 | mA | |
| P _s | Safety input, output, or total power | R _{θJA} =100°C/W, T _J =150°C, T _A =25°C | Input side | 50 | mW |
| | | | Output side | 1200 | |
| | | | Total | 1250 | |
| T _s | Maximum safety temperature | | 150 | °C | |

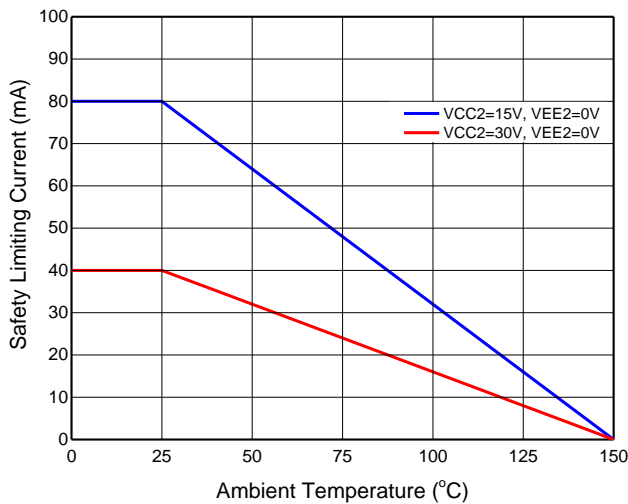


Figure 3. Thermal Derating Curve for Limiting Current per VDE

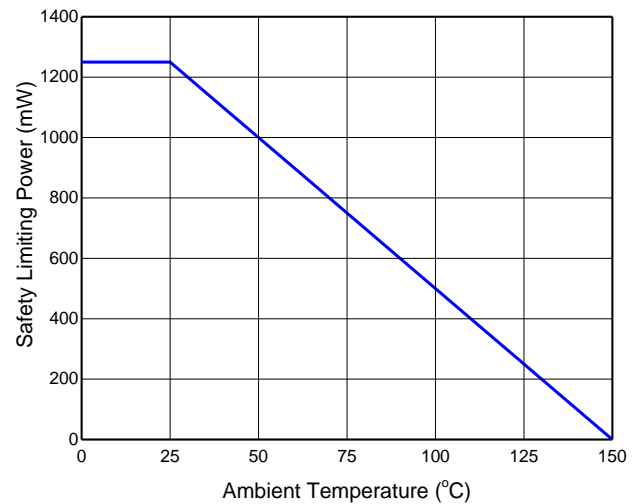


Figure 4. Thermal Derating Curve for Limiting Power per VDE

ELECTRICAL CHARACTERISTICS (DC)

All typical values at VCC1-GND1 = 5V, VCC2-GND2 = 15V, VEE2-GND2 = -8V and T_A = 25°C unless otherwise specified. All min and max specifications are at recommended operating conditions and T_A = -40°C to 125°C.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|------------------------------|--|------------------------------------|------|------|------|------|
| Under Voltage Lockout | | | | | | |
| V _{UVLO1_R} | Under Voltage Lockout Rising on VCC1 | | | 2.7 | 2.95 | V |
| V _{UVLO1_F} | Under Voltage Lockout Falling on VCC1 | | 2.3 | 2.5 | | V |
| V _{UVLO1_HYS} | Under Voltage Lockout Hysteresis on VCC1 | | | 0.2 | | V |
| V _{UVLO2_R} | Under Voltage Lockout Rising on VCC2 | | 10.5 | 11.7 | 13 | V |
| V _{UVLO2_F} | Under Voltage Lockout Falling on VCC2 | | 9.5 | 10.8 | 12 | V |
| V _{UVLO2_HYS} | Under Voltage Lockout Hysteresis on VCC2 | | | 0.9 | | V |
| Quiescent Current | | | | | | |
| I _{VCC1QL} | VCC1 Quiescent Current | IN+ = GND1, IN- = VCC1 | | 3.5 | 6 | mA |
| I _{VCC2QL} | VCC2 Quiescent Current | IN+ = GND1, IN- = VCC1 | | 5.5 | 10 | mA |
| I _{VCC1QH} | VCC1 Quiescent Current | IN+ = VCC1, IN- = GND1 | | 6 | 11 | mA |
| I _{VCC2QH} | VCC2 Quiescent Current | IN+ = VCC1, IN- = GND1 | | 6.5 | 12 | mA |
| Logic IOs | | | | | | |
| V _{INH} | Input High Threshold (IN+, IN-, RST) | | | | 70% | VCC1 |
| V _{INL} | Input Low Threshold (IN+, IN-, $\overline{\text{RST}}$) | | 30% | | | VCC1 |
| V _{IN_HYS} | Input Hysteresis (IN+, IN-, $\overline{\text{RST}}$) | | | 15% | | VCC1 |
| I _{IH} | High Level Input Leakage (IN+, RST) | IN+=VCC1, RST =VCC1, | 70 | 100 | 150 | uA |
| I _{IL} | Low Level Input Leakage (IN-) | IN-=GND1 | -150 | -100 | -70 | uA |
| V _{OL} | Low Level Output Voltage (FLT , RDY) | I=5mA | | 100 | 200 | mV |
| Driver Stage | | | | | | |
| I _{OUTH} | High Level Peak Output Current | IN+=VCC1, IN- =GND1, VOUT=VCC2-15V | 7 | 12 | | A |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-------------------------------|---|--|------|------|------|------|
| I _{OUTL} | Low Level Peak Output Current | IN+=GND1, IN-=VCC1, VOUT=VEE2+15V | 7 | 12 | | A |
| V _{OH} | High Level Output Voltage | IN+=VCC1, IN-=GND1, I _o =-100mA | | 45 | 90 | mV |
| V _{OL} | Low Level Output Voltage | IN+=GND1, IN-=VCC1, I _o =100mA | | 35 | 70 | mV |
| V _{OUTPD} | Active Output Pulldown Voltage | I _{OUTH/L} =200mA, VCC2 open | | | 2.3 | V |
| Miller Clamp | | | | | | |
| V _{CLPTH} | Clamp threshold voltage | | 1.8 | 2 | 2.2 | V |
| V _{CLP} | Clamp low level voltage | IN+=GND1, IN-=VCC1, I _{CLMPI} =200mA | | 100 | 200 | mV |
| I _{CLP} | Clamp low sink current | IN+=GND1, IN-=VCC1, V _{CLMPI} =VEE2+2.5V | 2 | 4 | | A |
| Short Circuit Clamping | | | | | | |
| V _{CLP-OUTH} | Clamping Voltage (OUTH – VCC2) | IN+=GND1, IN-=VCC1, I _{OUTH} = 500mA, t _{CLP} =10us | | 0.9 | 1.1 | V |
| V _{CLP-OUTL} | Clamping Voltage (OUTL – VCC2) | IN+=VCC1, IN-=GND1, I _{OUTL} = 500mA, t _{CLP} =10us | | 1.1 | 1.4 | V |
| V _{CLP-CLMPI} | Clamping Voltage (CLMPI – VCC2) | IN+=VCC1, IN-=GND1, I _{CLMPI} = 500mA, t _{CLP} =10us | | 1.2 | 1.5 | V |
| DESAT Protection | | | | | | |
| I _{CHG} | blanking capacitor charge current | DESAT-GND2=2V | 0.38 | 0.48 | 0.58 | mA |
| I _{DCHG_DESAT} | blanking capacitor discharge current | DESAT-GND2=6V | 9 | 14 | 19 | mA |
| V _{DSTH} | DESAT threshold voltage with respect to GND2 | | 8 | 9 | 10 | V |
| V _{DSSL} | DESAT voltage with respect to GND2 when OUTH/L is low | I _{DESAT} =1mA | | | 0.8 | V |
| Soft Turn-Off | | | | | | |
| I _{OLF} | Low Level output current during fault condition (soft turn off) | | 300 | 550 | 800 | mA |

SWITCHING CHARACTERISTICS (AC)

All typical values at VCC1-GND1 = 5V, VCC2-GND2 = 15V, VEE2-GND2 = -8V and T_A = 25°C unless otherwise specified. All min and max specifications are at recommended operating conditions and T_A = -40°C to 125°C

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------------------------|--|---|-----|------|------|-------|
| t _{PLH} | Propagation delay, Low to High | C _{LOAD} =1nF, f _{sw} =20kHz, (50% Duty Cycle), V _{CC2} =15V | | 90 | 130 | ns |
| t _{PHL} | Propagation delay, High to Low | | | 90 | 130 | ns |
| t _{PWD} | Pulse Width Distortion | | | | 35 | ns |
| t _{sk-pp} | Part to Park skew | | | | 35 | ns |
| t _r | Turn on rise time | C _{LOAD} =10nF, V _{CC2} =15V, V _{EE2} =GND2=0V | | 28 | | ns |
| t _f | Turn off fall time | | | 23 | | ns |
| t _{UVLO1_REC} | VCC1 UVLO Recovery Delay | VCC1 Rising from 0V to 5V | | 15 | 25 | us |
| t _{UVLO2_REC} | VCC2 UVLO Recovery Delay | VCC2 Rising from 0V to 15V | | 40 | 60 | us |
| t _{VCC1+_RDY} | VCC1 UVLO to RDY high Delay | VCC1 Rising from 0V to 5V | | 15 | 25 | us |
| t _{VCC2+_RDY} | VCC2 UVLO to RDY high Delay | VCC2 Rising from 0V to 15V | | 40 | 60 | us |
| t _{VCC2-_RDY} | VCC2 UVLO to RDY low Delay | VCC2 Falling from 15V to 0V | | 220 | | ns |
| t _{GF} | IN+, IN- signal glitch filter | | 20 | 30 | 40 | ns |
| t _{DESAT(90%)} | DESAT to 90% V _{OUT} Delay | C _{LOAD} =10nF | | 0.35 | 0.6 | us |
| t _{DESAT(10%)} | DESAT to 10% V _{OUT} Delay | C _{LOAD} =10nF | | 0.62 | 0.9 | us |
| t _{DESAT(MUTE)} | DESAT Fault Mute Time | | | 26 | 35 | us |
| t _{DESAT(GF)} | DESAT glitch filter delay | | | 0.15 | 0.25 | us |
| t _{DESAT(FLT)} | DESAT Fault to $\overline{\text{FLT}}$ Low Delay | | | 0.45 | 0.7 | us |
| t _{DESAT(RDY)} | DESAT Fault to RDY Low Delay | | | 0.45 | 0.7 | us |
| t _{DESAT(LEB)} | DESAT leading edge blanking time | | | 0.25 | 0.45 | us |
| t _{GFRST} | Glitch filter on $\overline{\text{RST}}$ for resetting $\overline{\text{FLT}}$ | | | 0.2 | 0.3 | us |
| CMT _{IH} | Output High Level Common Mode Transient Immunity | V _{CM} =1500V, V _{CC2} =15V, T _A =25°C | 150 | | | kV/us |
| CMT _{IL} | Output Low Level Common Mode Transient Immunity | V _{CM} =1500V, V _{CC2} =15V, T _A =25°C | 150 | | | kV/us |

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A=25^{\circ}\text{C}$, $V_{CC1-GND1} = 5\text{V}$, $V_{CC2-GND2} = 15\text{V}$, $V_{EE2}=GND2$, $C_{LOAD}=1\text{nF}$, unless otherwise specified

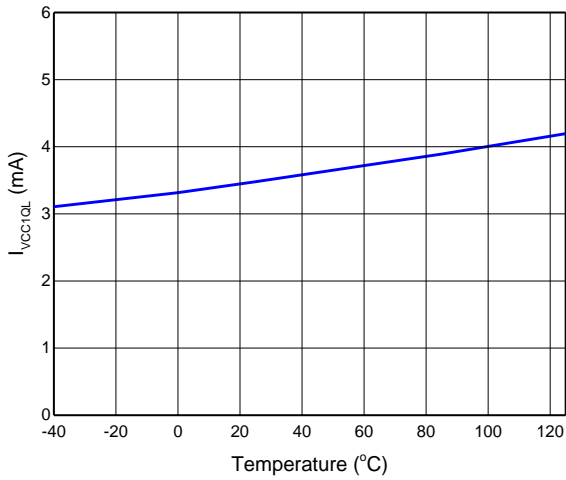


Figure 5. I_{VCC1QL} vs Temperature

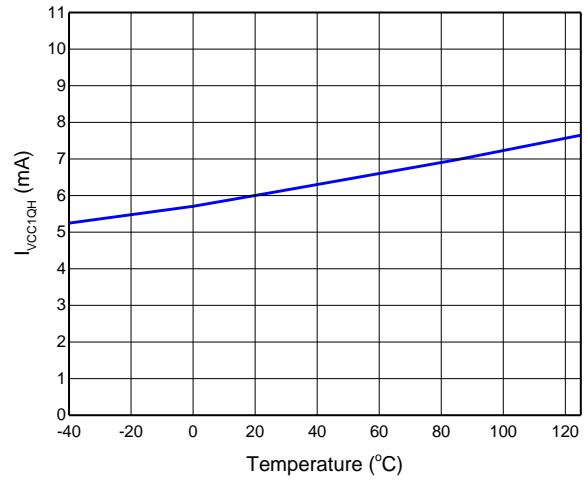


Figure 6. I_{VCC1QH} vs Temperature

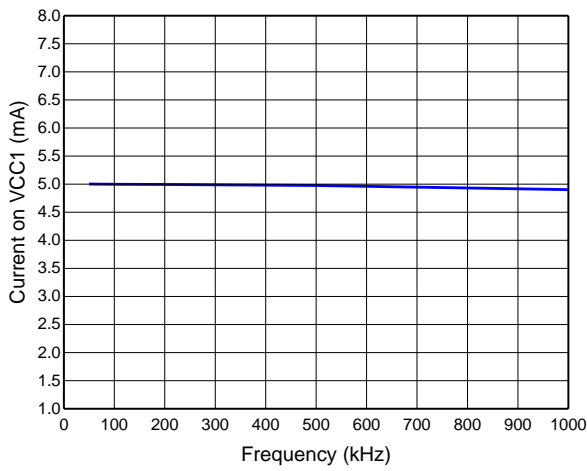


Figure 7. I_{VCC1} vs Frequency

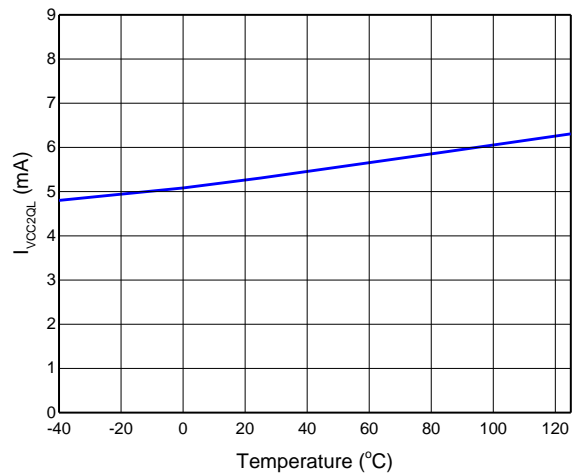


Figure 8. I_{VCC2QL} vs Temperature

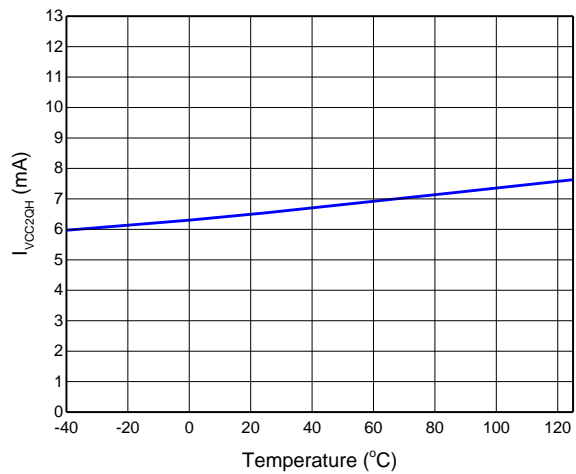


Figure 9. I_{VCC2QH} vs Temperature

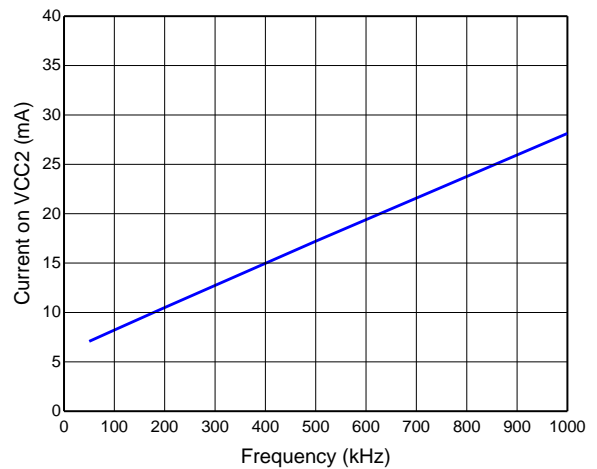


Figure 10. I_{VCC2} vs Frequency

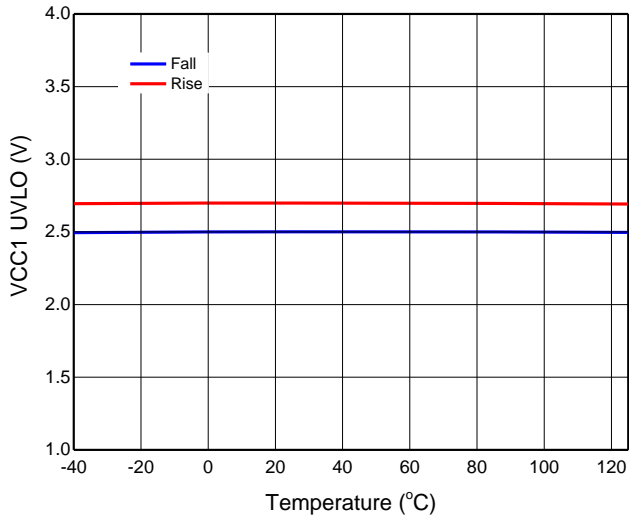


Figure 11. VCC1 UVLO vs Temperature

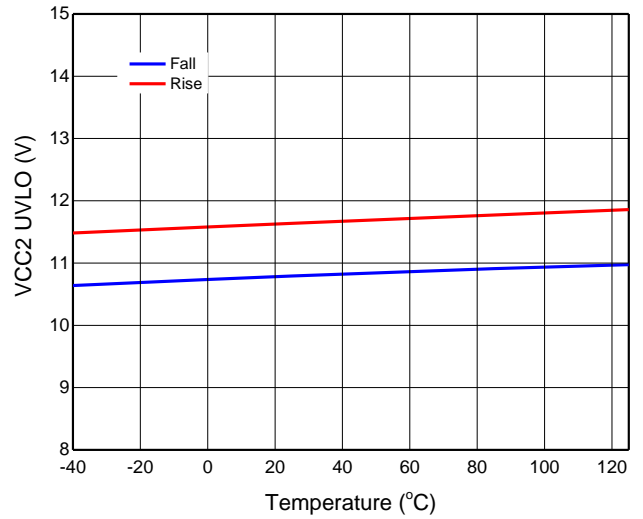


Figure 12. VCC2 UVLO vs Temperature

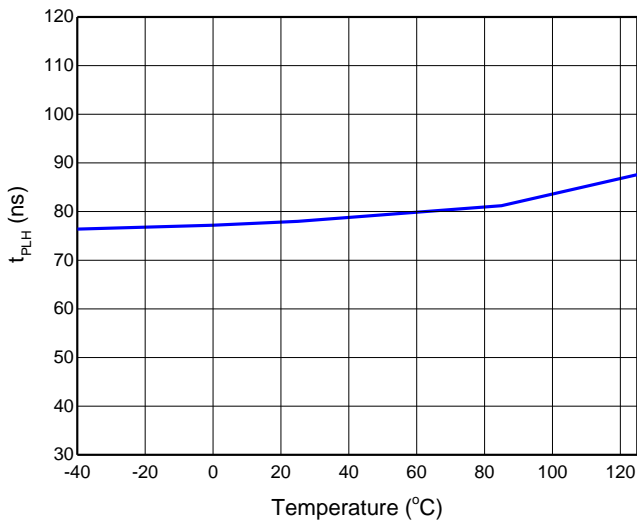


Figure 13. Propagation delay t_{PLH} vs Temperature

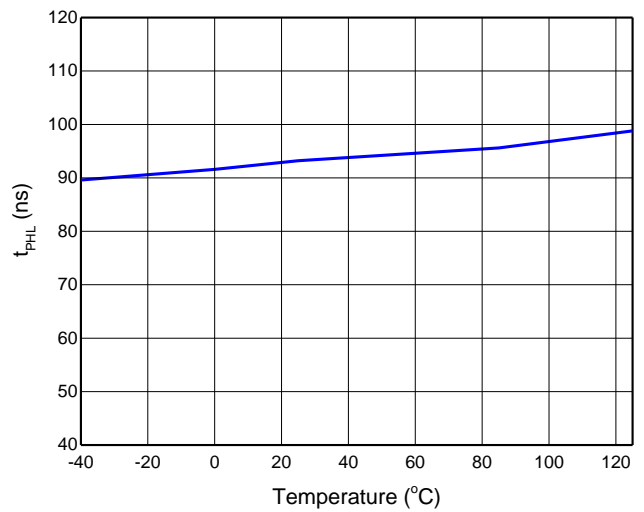


Figure 14. Propagation delay t_{PHL} vs Temperature

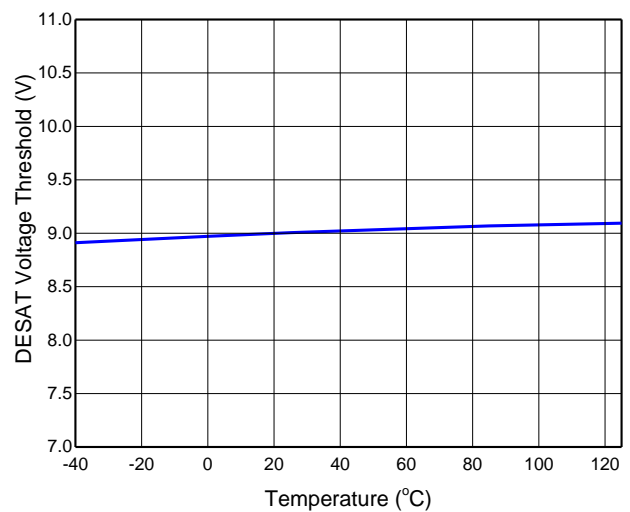
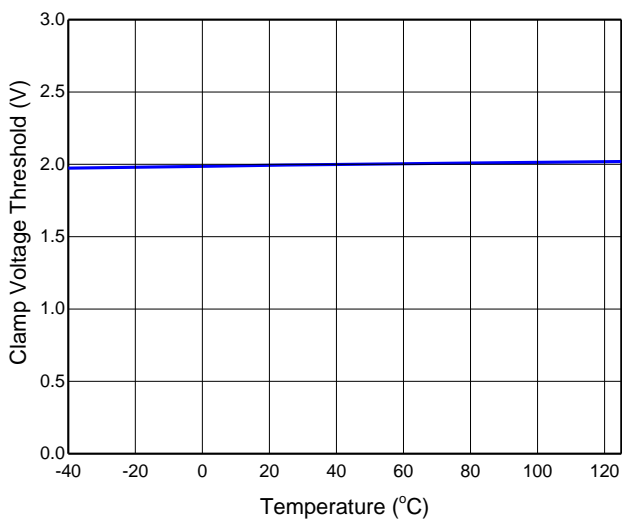


Figure 15. Clamp threshold voltage vs Temperature

Figure 16. Desat threshold voltage vs Temperature

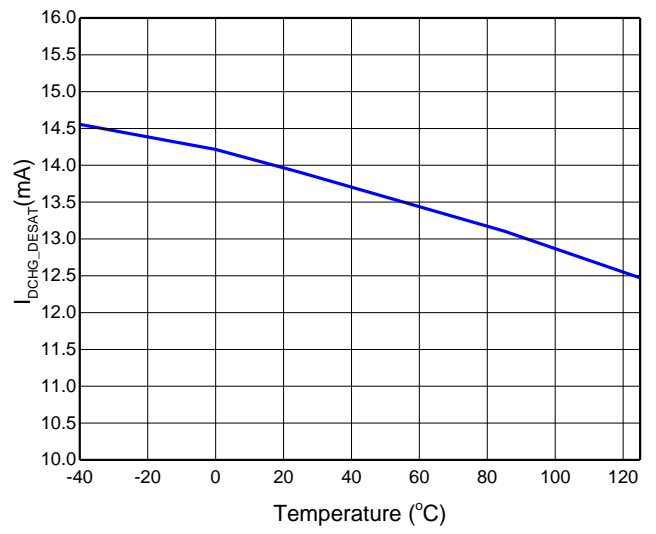
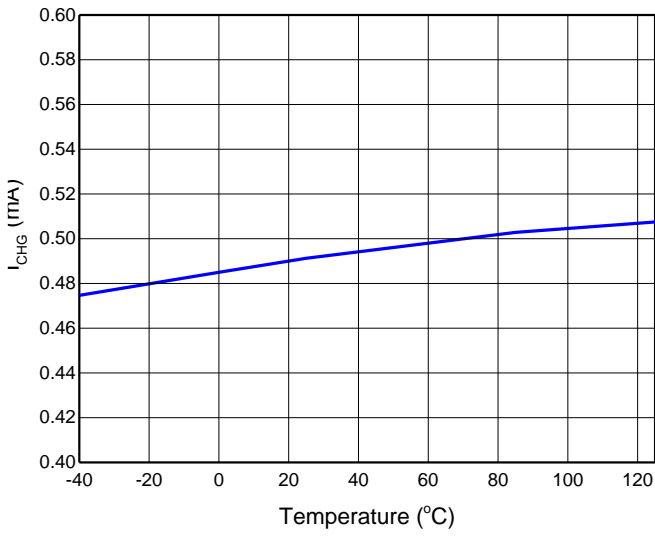


Figure 17. I_{CHG} vs Temperature

Figure 18. I_{DCHG_DESAT} vs Temperature

PARAMETER MEASUREMENT INFORMATION

Propagation Delay, Rise Time and Fall Time

Figure 19 and Figure 20 shows the circuit used to measure the rise (t_r) and fall (t_f) times, and the propagation delays t_{PDH} and t_{PDHL} .

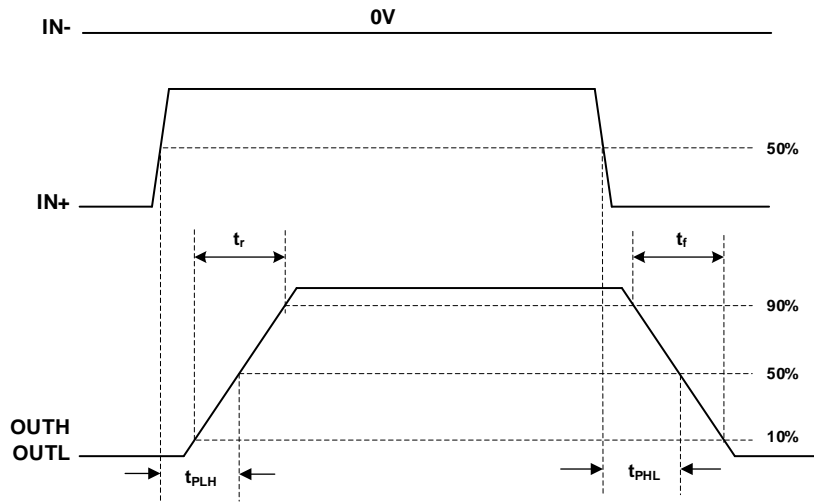


Figure 19. Propagation Delay, Rise Time and Fall Time in Noninverting Configuration

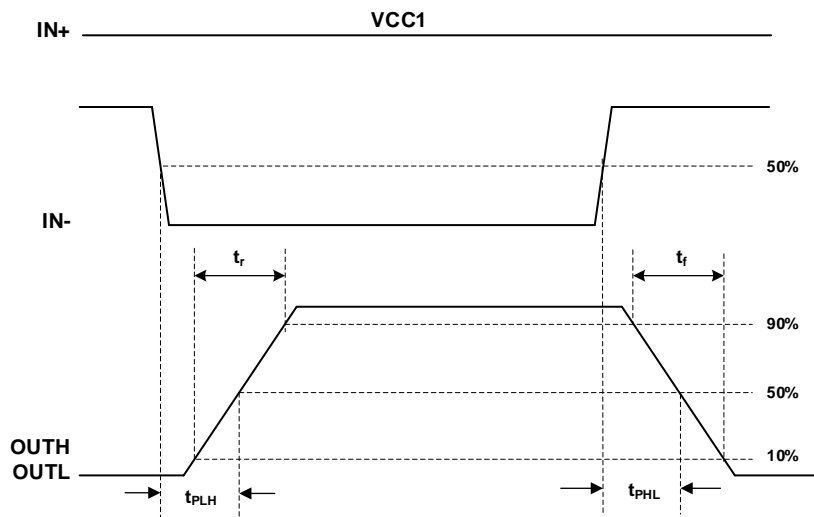


Figure 20. Propagation Delay, Rise Time and Fall Time in Inverting Configuration

CMTI Testing

Figure 21 to Figure 24 show the simplified diagram of the CMTI testing configuration.

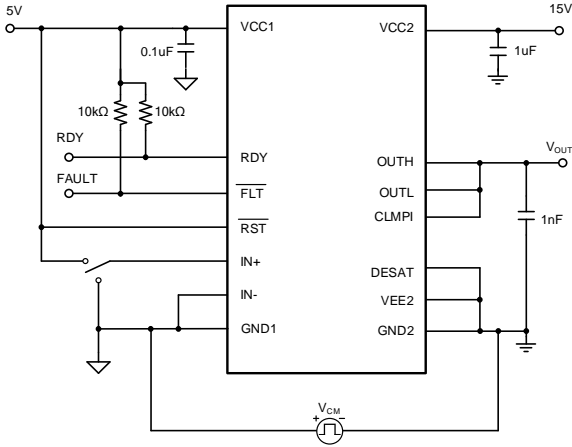


Figure 21. CMTI Test for Output

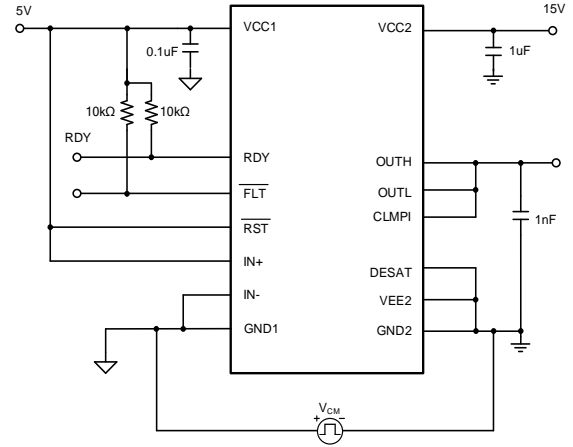


Figure 22. CMTI Test for RDY

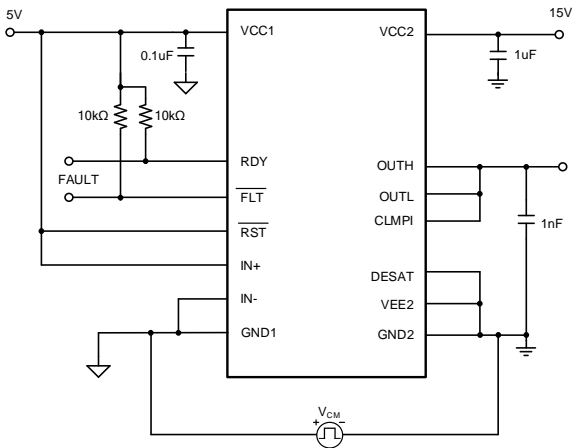


Figure 23. CMTI Test for Fault High

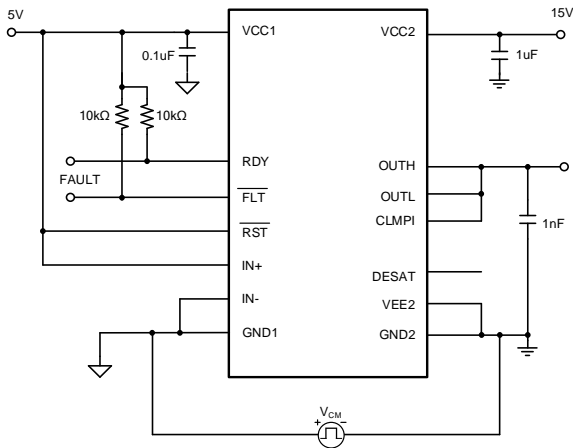


Figure 24. CMTI Test for Fault Low

Input Glitch Filter Testing

Figure 25 and Figure 26 show the IN+ pin pulse deglitch filter timing and Figure 27 and Figure 28 show the IN- pin pulse deglitch filter timing.

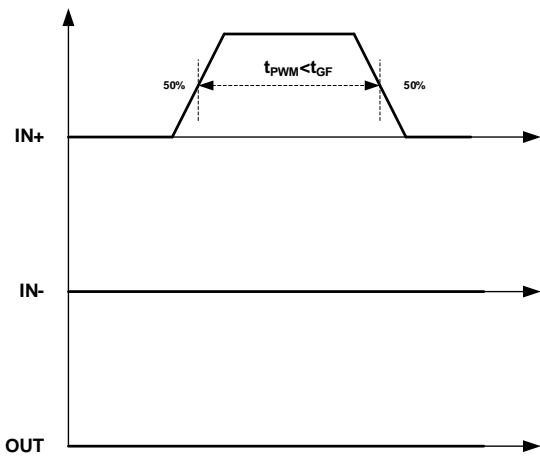


Figure 25. IN+ On Deglitch Filter

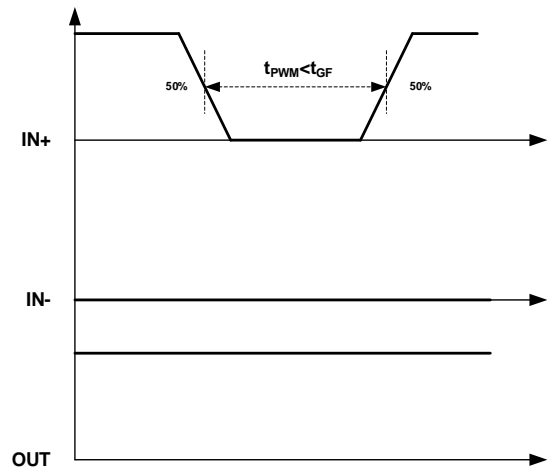


Figure 26. IN+ Off Deglitch Filter

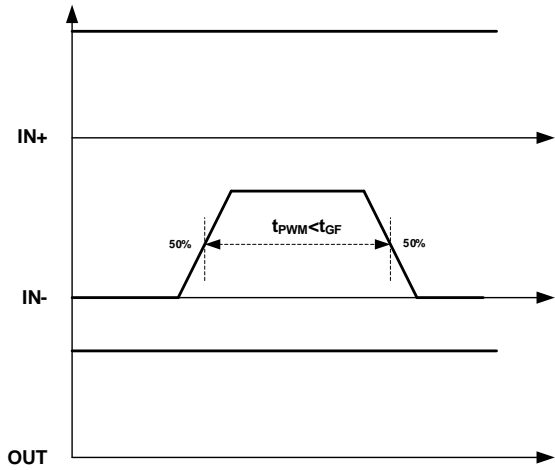


Figure 27. IN- On Deglitch Filter

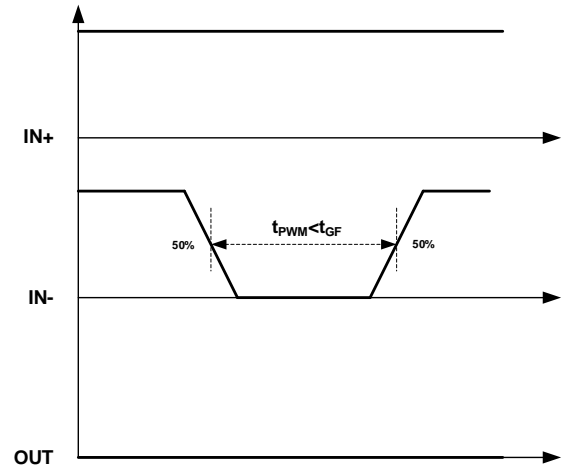


Figure 28. IN- Off Deglitch Filter

FEATURE DESCRIPTION

The SiLM5992SH-AQ is an advanced input CMOS logic single channel isolated gate driver with rich protection features, such as desaturation detection, miller clamp, isolated fault sensing and under voltage lockout.

UVLO with RDY Pin Indication

The IGBT is turned off if either supply VCC1 or VCC2 drops below UVLO threshold irrespective to other logic control signals. RDY pin indicates status of input and output side UVLO internal protection feature. If either side of device have insufficient supply (VCC1 or VCC2), the RDY pin output goes low; otherwise, RDY pin output is high. RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

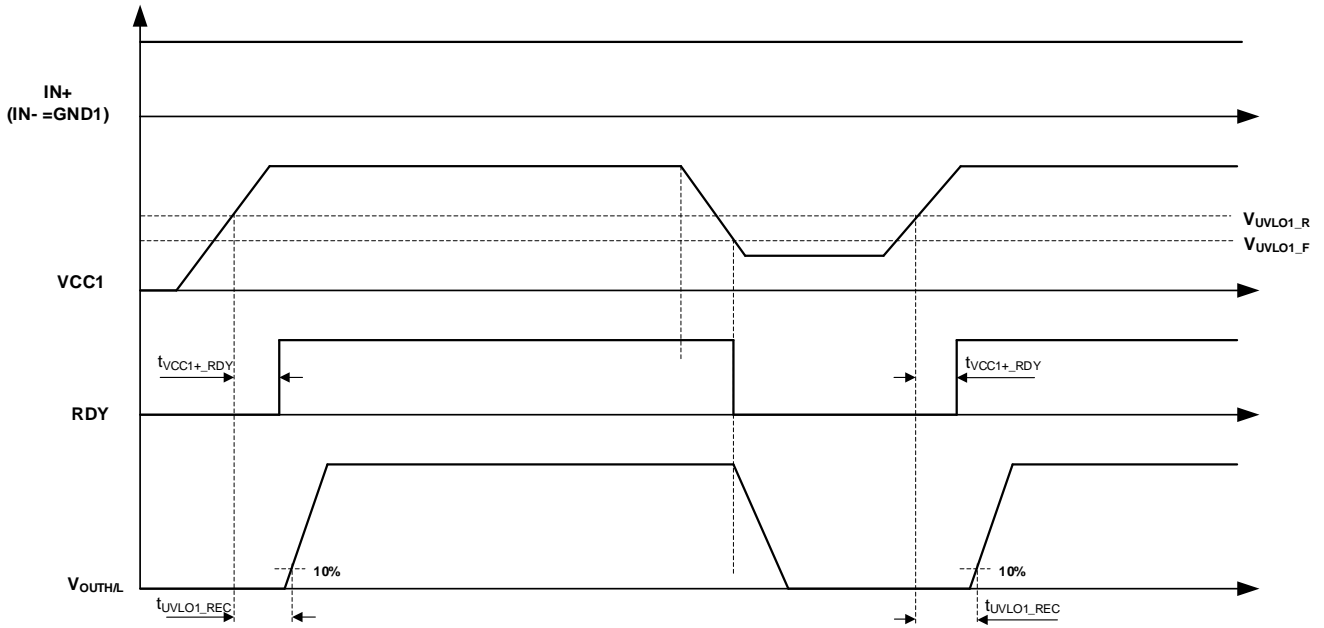


Figure 29.VCC1 UVLO Protection Timing

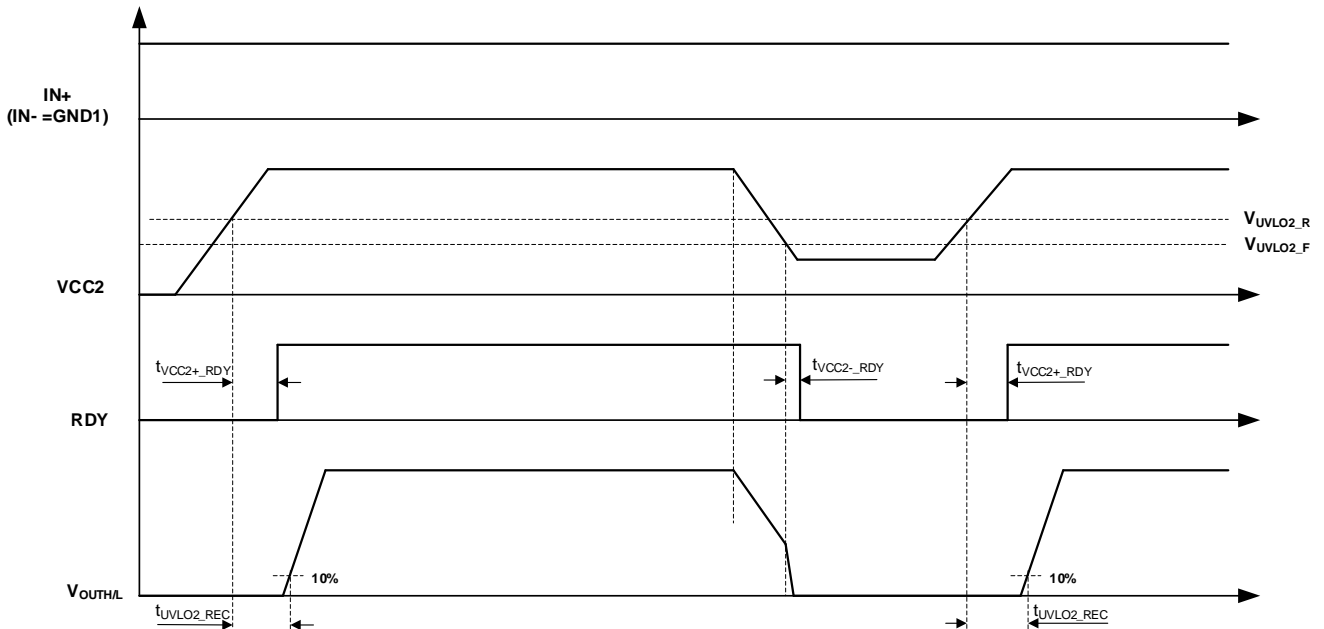


Figure 30.VCC2 UVLO Protection Timing

Fault Sensing and Reset

The SiLM5992SH-AQ integrates isolated fault indication. When the DESAT has monitored a fault on the IGBT, it also activates an internal feedback channel which pull low the FLT and RDY pin in the input side to inform the fault condition to a micro-controller. In the meanwhile, all input control signals will be ignored during the fault period to allow the driver to completely soft shutdown the IGBT. The driver will automatically reset the RDY pin after a fixed mute time, $t_{DESAT(MUTE)}$. The FLT output condition is latched and can only be reset after RDY goes high, through an active-low pulse at the RST input. RST has an internal filter to reject noise and glitches. By asserting RST for at least the specified minimum duration, t_{GFRST} , the device input logic can be enabled or disabled.

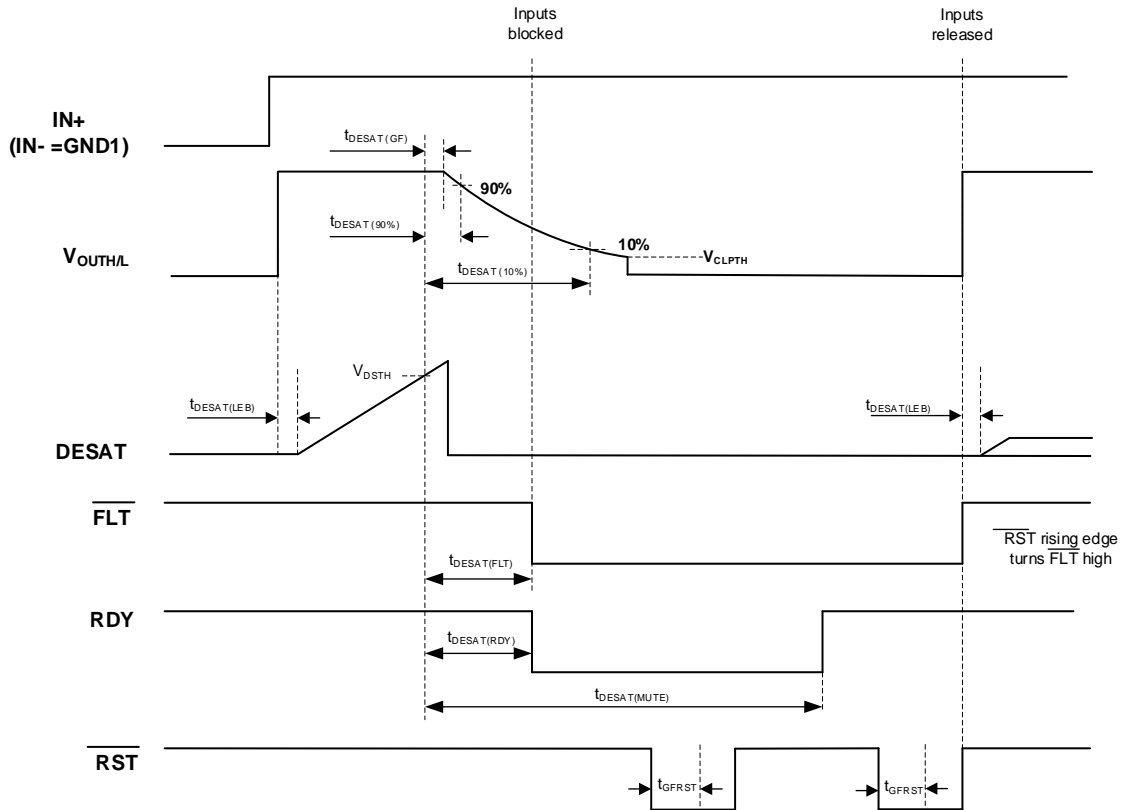


Figure 31. FLT , RDY and RST Timing Diagram

Desaturation Detection

The DESAT pin monitors the IGBT V_{CE} voltage. When the voltage on the DESAT pin exceeds DESAT threshold 9V while the IGBT is on, a weak pull down circuit in the output driver stage will turn on to ramp down the V_{OUT} slowly and “softly” turn off the IGBT. This “softly” turn-off feature prevents large di/dt which induces high voltage spikes to damage the IGBT.

A blank time is needed in the DESAT detection circuit following the turn on of the IGBT to allow the collector voltage to fall below the DESAT threshold. The blank time is controlled by the internal DESAT blank charge current, the DESAT voltage threshold, and the external DESAT capacitor. Using the following equation to calculate the blank time.

$$t_{BLANK} = \frac{C_{BLANK} \times V_{DSTH}}{I_{CHG}}$$

Here:

- t_{BLANK} : Blank time
- C_{BLANK} : External DESAT capacitor
- V_{DSTH} : DESAT threshold voltage
- I_{CHG} : Blank capacitor charging current

During the IGBT turn on, high negative spike voltage occurs on the collection of the IGBT due to parasitic parameters and this negative spike may damage the DESAT pin. In order to protect the DESAT pin in such case, a resistor, R_{DST} , is needed to be in series with the DESAT diode. The value of the R_{DST} depends on the different application, but generally a 100Ω resistor is recommended. Further protection is possible through an optional Schottky diode to clamp the DESAT input to GND2 at low voltage levels with its low forward voltage.

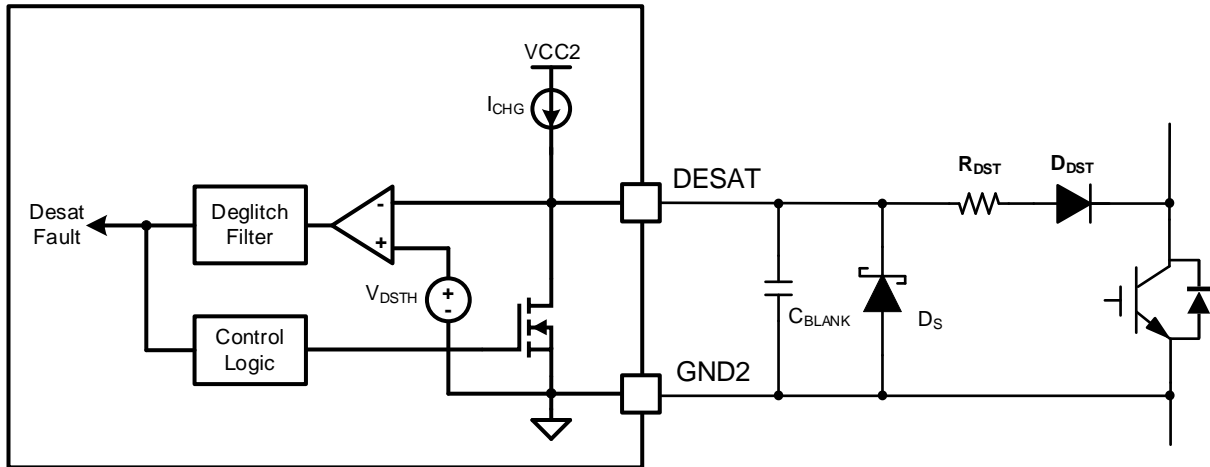


Figure 32. DESAT Protection

Soft Turn Off

SiLM5992SH-AQ initiates a soft turn-off when the short circuit protection is triggered. When the short circuit fault happens, the IGBT transits from the active region to the desaturation region very fast. The channel current is controlled by the gate voltage and decreasing in a soft manner, thus the overshoot of the IGBT is limited and prevents the overvoltage breakdown. The turn off speed needs to be slow to limit the overshoot voltage, but the shutdown time should not be too long that the large energy dissipation can breakdown the device. The 550mA soft turn off current of SiLM5992SH-AQ makes sure the power switches are safely turned off during short circuit events.

Internal Active Miller Clamp

A Miller clamp circuit integrates in the SiLM5992SH-AQ which allows the control of the Miller current during a high dV/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn off, the gate voltage is monitored through the OUTH pin and the clamp circuit is activated when the voltage on the OUTH pin goes below the clamp voltage threshold, V_{CLMTH} (2V typical, relative to VEE2). A clamp low sink current is generated when the clamp circuit is activated. The clamp circuit is disabled when the input on signal is triggered again. In order to achieve good clamping results, the CLMPI shall connect to the gate of the power device, close to the power device on the PCB layout.

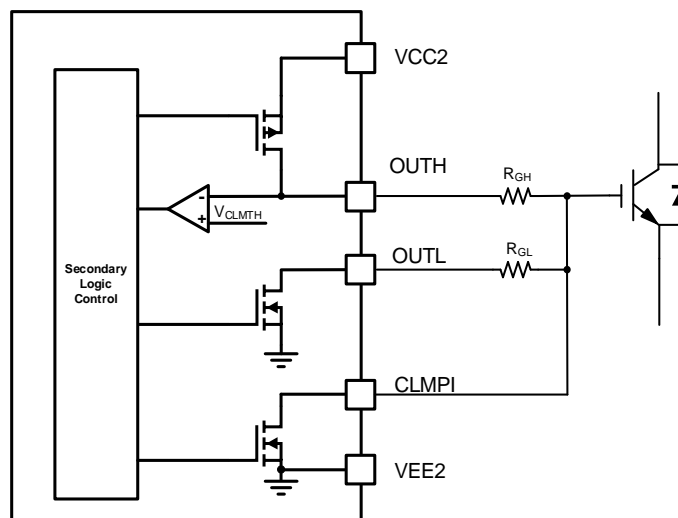


Figure 33. Active Miller Clamp

Active Output Pulldown

The Active output pulldown feature ensures that the IGBT gate OUTH/L is clamped to VEE2 to ensure safe IGBT off-state, when VCC2 is open.

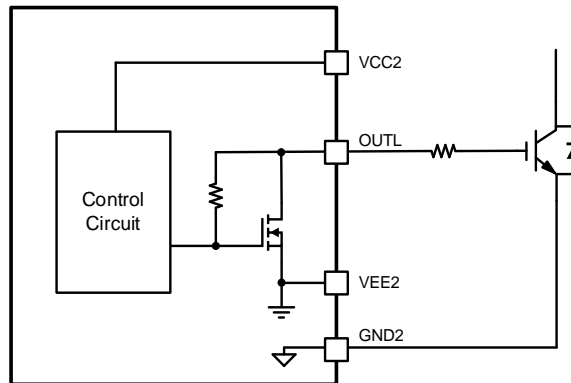


Figure 34. Active Output Pulldown

Short Circuit Clamping

Under short circuit events it is possible that currents are induced back into the gate-driver OUTH/L and CLMPI pins due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUTH/L and CLMPI help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, such as, a t_{GF} deglitch filter on IN+, IN- and, a t_{GFRST} deglitch filter on \overline{RST} is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN- PWM pulse is smaller than the input deglitch filter width, there will be no responses on drive signal.

Device Functional Modes

Table 1. SiLM5992 function table

| VCC1 | VCC2 | VEE | IN+ | IN- | \overline{RST} | RDY | \overline{FLT} | OUTH/OUTL | CLMPI |
|------|------|-----|------|------|------------------|-----|------------------|-----------|-------|
| PU | PD | PU | X | X | X | Low | HiZ | Low | Low |
| PD | PU | PU | X | X | X | Low | HiZ | Low | Low |
| PU | PU | PU | X | X | Low | HiZ | HiZ | Low | Low |
| PU | PU | PU | Low | X | High | HiZ | HiZ | Low | Low |
| PU | PU | PU | X | High | High | HiZ | HiZ | Low | Low |
| PU | PU | PU | High | Low | High | HiZ | HiZ | High | HiZ |

PU: Power up, voltage higher than UVLO, PD: Power down, voltage lower than UVLO, HiZ, High impedance

LAYOUT

In order to achieve optimum performance for the SiLM5992SH-AQ, some suggestions on the PCB layout.

Component placement:

- Low-ESR capacitors must be connected close to the device between the V_{CC2} and V_{EE} pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the V_{EE} pins connected to the switch node, the parasitic inductances between the source of the top transistor and the drain of the bottom transistor must be minimized.

Grounding considerations:

- Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. Small trace loop decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

High-voltage considerations:

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

PACKAGE CASE OUTLINES

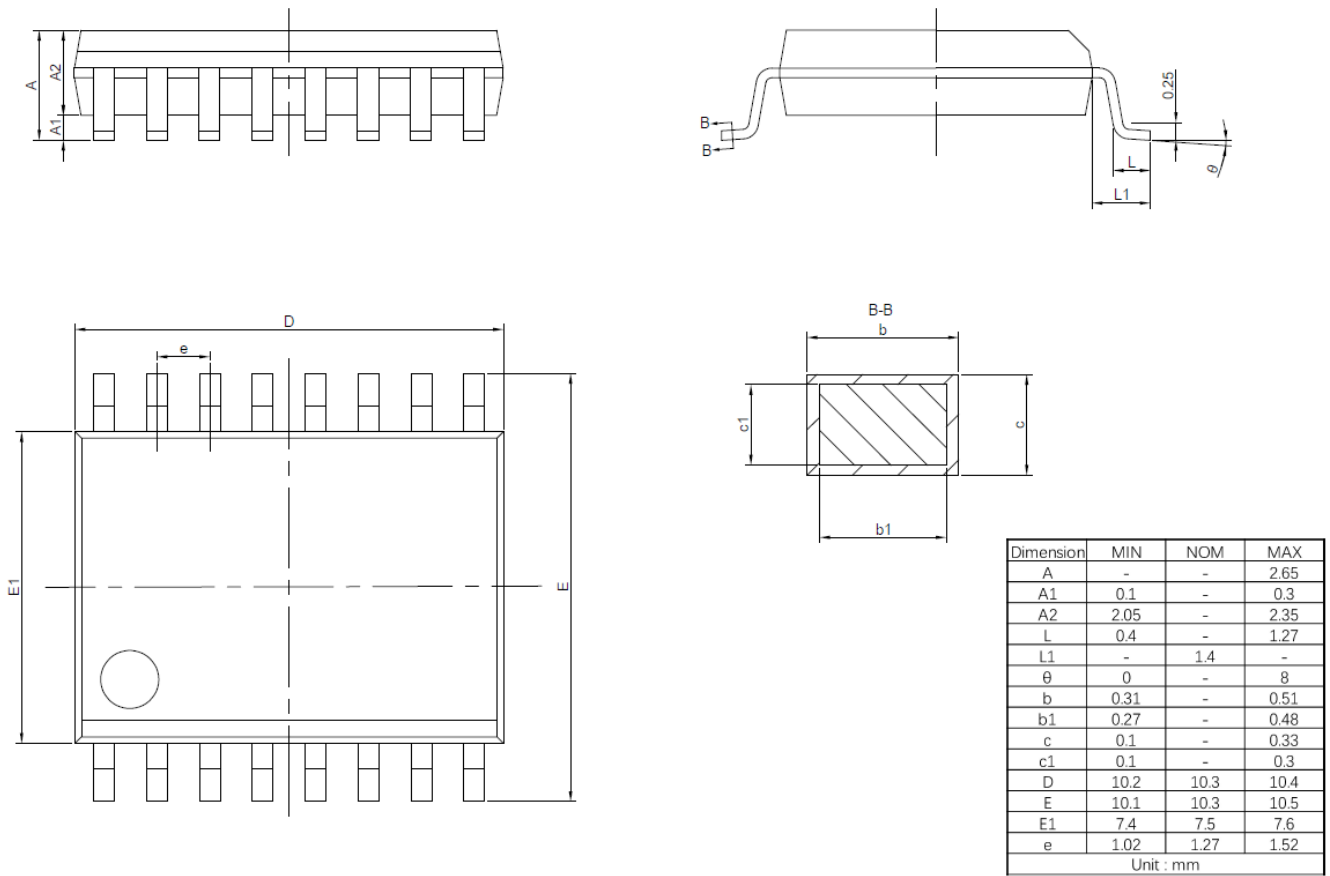


Figure 35. SOP16W Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

| Page or Item | Subjects (major changes since previous revision) |
|--------------------------------------|---|
| Rev 1.0 datasheet: 2023-08-17 | |
| Whole document | Initial datasheet release |