Isolated CAN Transceiver with Fault Protection and CAN FD

GENERAL DESCRIPTION

The SiLM5144S is a galvanic isolated high speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high speed CAN specification. The SiLM5144S transceiver supports both classical CAN and CAN FD (Flexible Data Rate) networks up to 5 megabits per second (Mbps). The SiLM5144S transceiver also includes many protections and diagnostic features including thermal-shutdown (TSD), TXD-dominant time-out (DTO), supply under-voltage detection, and bus fault protection up to ±65 V.

The device uses a silicon dioxide insulation barrier with a withstand voltage of 3000V_{RMS}.

APPLICATION

- Battery Management System
- DC/DC Converter
- On-Board and wireless charger
- Inverter and motor control

FEATURES

- Meets the requirements of ISO 11898-2:2016 physical layer standards
- Support of classical CAN and optimized CAN FD performance up to 5Mbps
- Low loop delay of 150ns
- Receiver Common Mode Input Voltage in Normal Mode: ±30 V
- Protection features
  - Bus fault protection: ±65 V
  - Under-voltage protection
  - TXD-dominant time-out (DTO)
  - Thermal-shutdown protection (TSD)
- High CMTI of 100kV/us
- VCC1 voltage range: 2.25V to 5.5V
- VCC2 voltage range: 4.5V to 5.5V
- Operation temperature, T_A: –40°C to +125°C
- Package: SOP8
- Safety certifications
  - 3kV_{RMS} isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2022
  - DIN VDE 0884-17: 2021-10 (Pending)

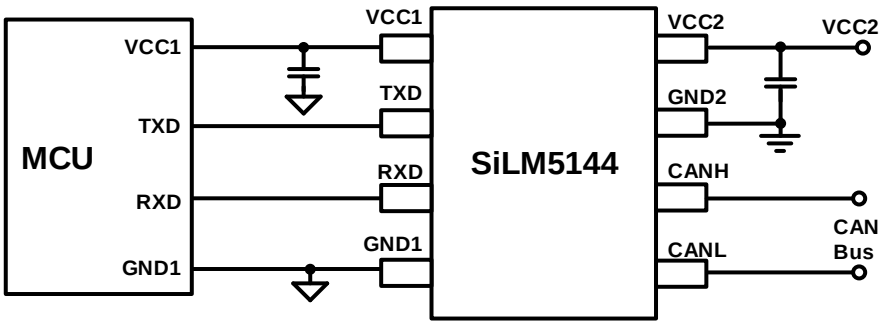

Figure 1. SiLM5144S Application Circuit

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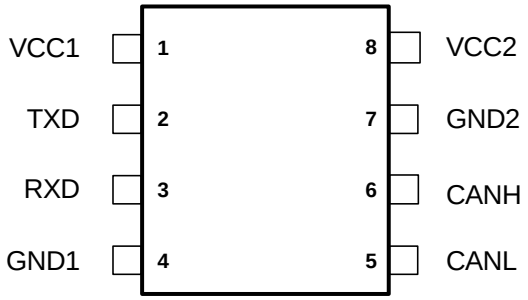
PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP8	

PIN DESCRIPTION

No.	Pin	Description
1	VCC1	Digital side supply voltage
2	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	GND1	Digital side ground
5	CANL	Low level CAN bus line
6	CANH	High level CAN bus line
7	GND2	Transceiver side ground
8	VCC2	Transceiver side supply voltage

FUNCTIONAL BLOCK DIAGRAM

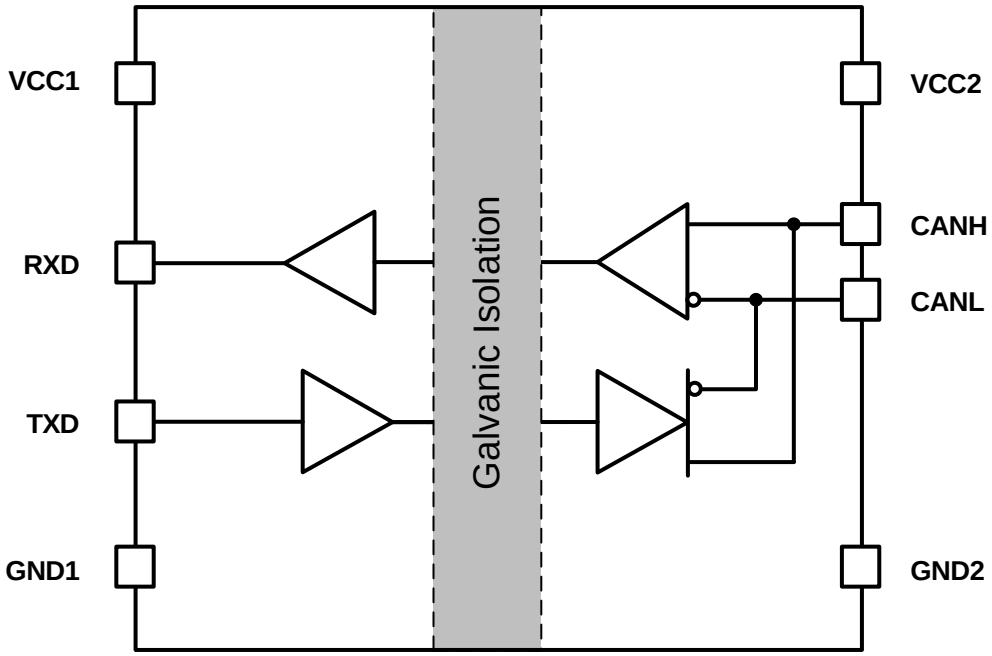


Figure 2. SiLM5144S Block Diagram

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM5144SCA-DG	SOP8, Pb-Free	2500/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Units
V_{CC1}	Digital Side Supply Voltage	-0.3	6	V
V_{CC2}	Transceiver Side Supply Voltage	-0.3	6	V
V_{BUS}	CANH, CANL Voltage	-65	65	V
V_{DIFF}	Max differential voltage between CANH and CANL	-65	65	V
V_I	Logic input voltage TXD	-0.3	V_{CC1}+0.3	V
V_O	Logic output voltage RXD	-0.3	V_{CC1}+0.3	V
I_{RXD}	RXD output current	-8	8	mA
T_J	Junction Temperature	-40	150	°C
T_S	Storage Temperature	-65	150	°C

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Max	Units
V_{CC1}	Digital Side Supply Voltage	2.25	5.5	V
V_{CC2}	Transceiver Side Supply Voltage	4.5	5.5	V
I_{RXD}	RXD output current	-2	2	mA
T_J	Junction Temperature	-40	150	°C
T_A	Ambient Temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM All Terminals	±4000	V
	HBM CANH and CANL to GND	±8000	V
	CDM	±2000	V

THERMAL INFORMATION

Symbol	Definition	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	135.3	°C/W
$R_{\theta JC}$	Junction to case (top) thermal resistance	48	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min	Typ	Max	Units
R_{IO}	Resistance (Input Side to Output Side)		$>10^{12}$		Ω
C_{IO}	Capacitance (Input Side to Output Side)		1		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value	Units
CLR	External clearance	Shortest terminal to terminal distance through air	>4	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	V
	Material Group		I	
	Overvoltage category	Rated mains voltages ≤150V_{RMS}	I-IV	
		Rated mains voltages ≤300V_{RMS}	I-III	
		Rated mains voltages ≤600V_{RMS}	I-II	
		Rated mains voltages ≤1000V_{RMS}	I-I	
DIN V VDE 0884-11(1)				
V_{IORM}	Maximum repetitive peak isolation voltage		1000	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (Sine wave)	707	V_{RMS}
		DC voltage	1000	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	60s	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.3 x V_{IOSM}	6000	V_{PK}
q_{pd}	Apparent charge	Method b2: $V_{pd(m)}$=1.875 x V_{IORM}, tm=1 s	≤5	pC
	Climatic Category		40/125/21	
	Pollution Degree		2	
UL1577				
V_{ISO}	Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	3000	V_{RMS}

Note1: Certification pending

SAFETY RELATED CERTIFICATIONS

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Basic Insulation, V_{IORM} = 1000 V_{PK} V_{IOTM} = 4242 V_{PK}	Single protection, 3000 V_{RMS}	Basic insulation, Altitude≤ 5000m
Certification Pending	File number: Pending	File number: CQC23001373092

ELECTRICAL CHARACTERISTICS (DC)

All typical values at V_{CC1} = 5V, V_{CC2} = 5V and T_A = 25°C, all min and max specifications are at recommended operating conditions and T_A = -40°C to 125°C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply Characteristics						
I_{CC1_DOM}	VCC1 Current, Normal mode (dominant)	TXD=0V, bus dominant		2.1	4	mA
I_{CC1_REC}	VCC1 Current, Normal mode (recessive)	TXD=V_{CC1}, bus recessive		0.9	2	mA
$I_{CC2\_DOM\_60}$	VCC2 Current, Normal mode (dominant)	TXD=0V, bus dominant, R_L=60Ω		47	75	mA
$I_{CC2\_DOM\_50}$	VCC2 Current, Normal mode (dominant)	TXD=0V, bus dominant, R_L=50Ω		52	80	mA
$I_{CC2\_REC\_60}$	VCC2 Current, Normal mode (recessive)	TXD=V_{CC1}, bus recessive, R_L=60Ω		1	2	mA
$I_{CC2\_BUS\_FLT}$	VCC2 Current, Normal mode (bus fault)	TXD=0V, CANH=CANL=+/-25V			125	mA
$V_{UV\_VCC1\_R}$	Under Voltage Lockout Rising on VCC1			2.05	2.25	V
$V_{UV\_VCC1\_F}$	Under Voltage Lockout Falling on VCC1		1.65	1.9		V
$V_{UV\_VCC1\_HYS}$	Under Voltage Lockout Hysteresis on VCC1			0.15		V
$V_{UV\_VCC2\_R}$	Under Voltage Lockout Rising on VCC2		4	4.2	4.4	V
$V_{UV\_VCC2\_F}$	Under Voltage Lockout Falling on VCC2		3.8	4	4.2	V
$V_{UV\_VCC2\_HYS}$	Under Voltage Lockout Hysteresis on VCC2			0.2		V
T_{TSD}	Thermal Shutdown Temperature			190		°C
T_{TSD_HYS}	Thermal Shutdown Hysteresis			15		°C
TXD and RXD Logic IOs						
V_{IH}	Input High Threshold on TXD		70%			V_{CC1}
V_{IL}	Input Low Threshold on TXD				30%	V_{CC1}
I_{IH}	High Level Input Leakage TXD	TXD = 5V			1	uA
I_{IL}	Low Level Input Leakage TXD	TXD = 0V	-10	-4		uA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage on RXD	I_{RXD}=-2mA, V_{CC1} = 5V	4.7	4.9		V
V_{OL}	Low Level Output Voltage on RXD	I_{RXD}=2mA, V_{CC1} = 5V		0.06	0.2	V
Driver Characteristics						
$V_{OCANH(DOM)}$	CANH Bus Output Voltage, Dominant	50Ω ≤ R_L ≤ 65Ω, TXD=0V	2.75		4.5	V
$V_{OCANL(DOM)}$	CANL Bus Output Voltage, Dominant	50Ω ≤ R_L ≤ 65Ω, TXD=0V	0.5		2.25	V
$V_{OCANH(REC)}$	CANH Bus Output Voltage, Recessive	R_L=Open, TXD=V_{CC1}	2	0.5 x V_{CC2}	3	V
$V_{OCANL(REC)}$	CANL Bus Output Voltage, Recessive	R_L=Open, TXD=V_{CC1}	2	0.5 x V_{CC2}	3	V
$V_{OD(DOM)}$	Differential Output Voltage, Dominant	50Ω ≤ R_L ≤ 65Ω, TXD=0V	1.5		3.0	V
$V_{OD(REC)}$	Differential Output Voltage, Recessive	R_L=Open, TXD=V_{CC1}	-50		50	mV
V_{SYM}	Output Symmetry, (V_{OCANH} + V_{OCANL}) / V_{CC2}	50Ω ≤ R_L ≤ 65Ω, TXD=V_{CC1} or 0V	0.9		1.1	V/V
V_{SYM_DC}	DC Output Symmetry, V_{CC2} - (V_{OCANH} + V_{OCANL})	50Ω ≤ R_L ≤ 65Ω, TXD=V_{CC1} or 0V	-0.4		0.4	V
I_{OSCH_DOM}	CANH Output Short Circuit Current, Dominant Normal Mode	CANH=-15V to 40V, CANL Open, TXD=0V	-115			mA
I_{OSCL_DOM}	CANL Output Short Circuit Current, Dominant Normal Mode	CANL=-15V to 40V, CANH Open, TXD=0V			115	mA
I_{OSC_REC}	Output Short Circuit Current, Recessive Normal Mode	CANH=CANL=-40V to 40V, TXD= V_{CC1}	-5		5	mA
Receiver Characteristics						
V_{CM}	Common Mode Range, Normal Mode		-30		30	V
V_{IT+}	Positive Going Input Threshold Voltage, Normal Mode	-30V<V_{CM}<30V			0.9	V
V_{IT-}	Negative Going Input Threshold Voltage, Normal Mode	-30V<V_{CM}<30V	0.5			V
V_{IT_HYS}	Hysteresis for Input Threshold Voltage, Normal Mode	-30V<V_{CM}<30V		0.1		V
R_{ID}	Differential Input Resistance		50		80	kΩ
R_{IN}	Input Resistance (CANH or CANL)		25		40	kΩ
$R_{IN(M)}$	Input Resistance Matching 1- $R_{IN(CANH)}$ / $R_{IN(CANL)}$		-1		1	%

SWITCHING CHARACTERISTICS (AC)

All typical values at V_{CC1} = 5V, V_{CC2} = 5V and T_A = 25°C, all min and max specifications are at recommended operating conditions and T_A = -40°C to 125°C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver output RXD, recessive to dominant	R_L=60Ω, C_L=100pF, C_{L_RXD}=15pF,	55	130	200	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver output RXD, dominant to recessive		70	150	210	ns
t_{PHR}	Driver propagation delay time, high TXD to driver recessive, dominant to recessive	R_L=60Ω, C_L=100pF	30		120	ns
t_{PLD}	Driver propagation delay time, low TXD to driver dominant, recessive to dominant	R_L=60Ω, C_L=100pF	25		120	ns
t_{SKP}	Pulse skew ($\lvert t_{PHR} - t_{PLD} \rvert$)	R_L=60Ω, C_L=100pF			35	ns
t_R	Differential output signal rise time	R_L=60Ω, C_L=100pF	20	40	60	ns
t_F	Differential output signal fall time	R_L=60Ω, C_L=100pF	10	30	50	ns
t_{TXD_DTO}	Dominant timeout	R_L=60Ω, C_L=100pF	1.2	2.4	3.8	ms
t_{PRH}	Receiver propagation delay time, driver recessive to RXD high, dominant to recessive	C_{L_RXD}=15pF	40		120	ns
t_{PDL}	Receiver propagation delay time, driver dominant to RXD low, recessive to dominant		35		120	ns
t_{R_RXD}	RXD output signal rise time			2		ns
t_{F_RXD}	RXD output signal fall time			2.5		ns
$t_{BIT(BUS)}$	Bit time on CAN bus output with $t_{BIT(TXD)}$ = 500ns	R_L=60Ω, C_L=100pF, C_{L_RXD}=15pF	435		530	ns
	Bit time on CAN bus output with $t_{BIT(TXD)}$ = 200ns		155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output with $t_{BIT(TXD)}$ = 500ns		400		550	ns
	Bit time on RXD output with $t_{BIT(TXD)}$ = 200ns		120		220	ns
Δt_{REC}	Receiver timing Symmetry $t_{BIT(TXD)}$ = 500ns	R_L=60Ω, C_L=100pF, C_{L_RXD}=15pF, Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$	-65		45	ns
	Receiver timing Symmetry $t_{BIT(TXD)}$ = 200ns		-45		15	ns

PARAMETER MEASUREMENT INFORMATION

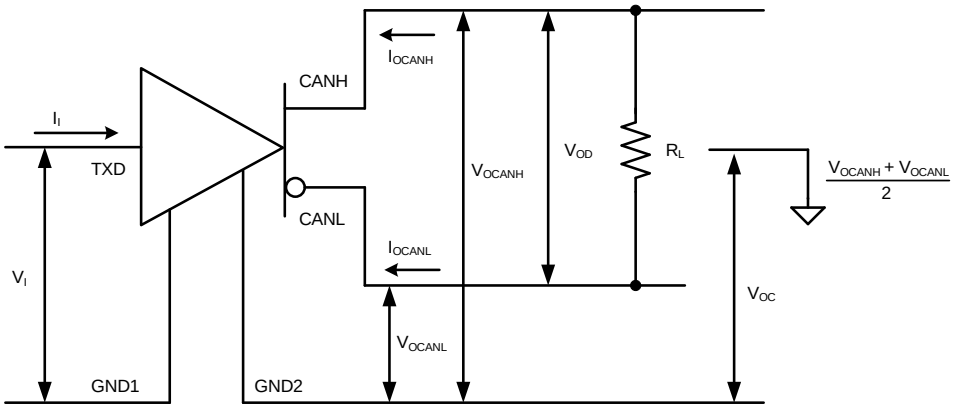


Figure 3. Driver Voltage and Current

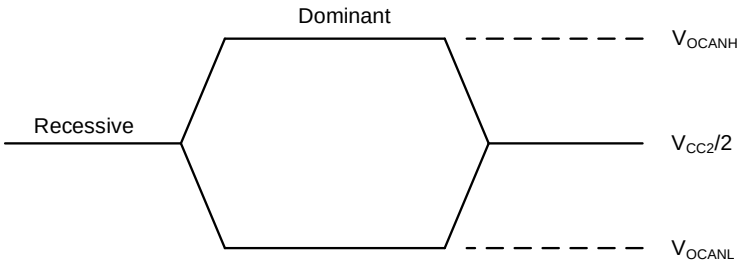


Figure 4. Bus Logic State Voltage Definition

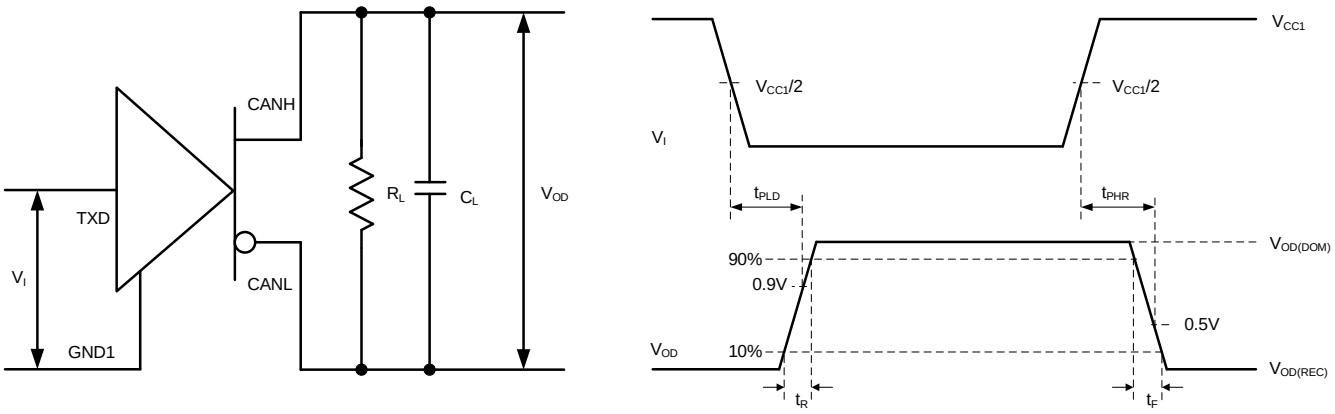


Figure 5. Driver Test Circuit and Timing

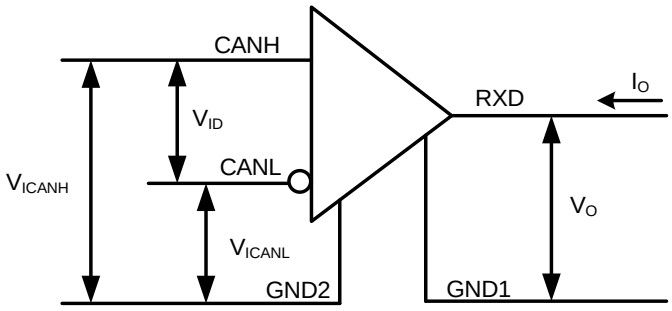


Figure 6. Receiver Voltage and Current

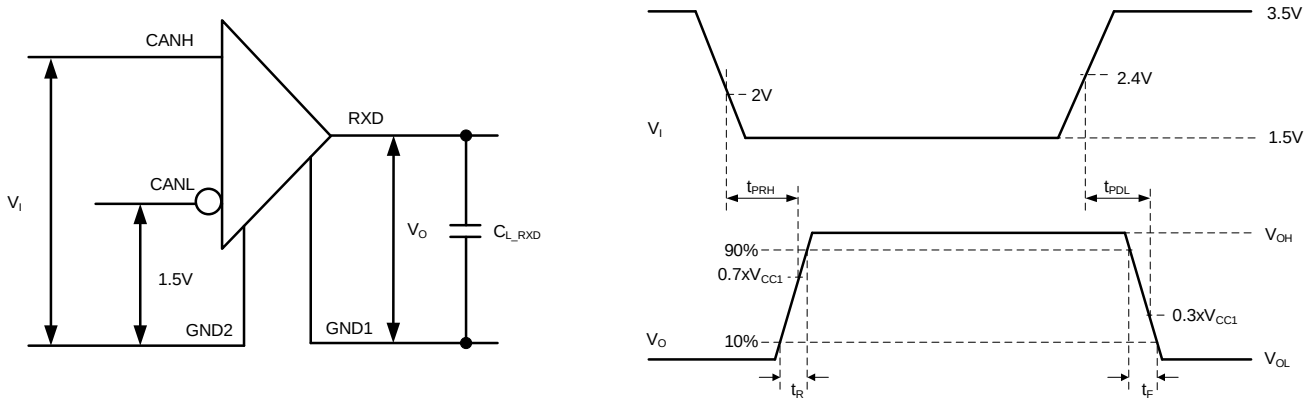


Figure 7. Receiver Test Circuit and Timing

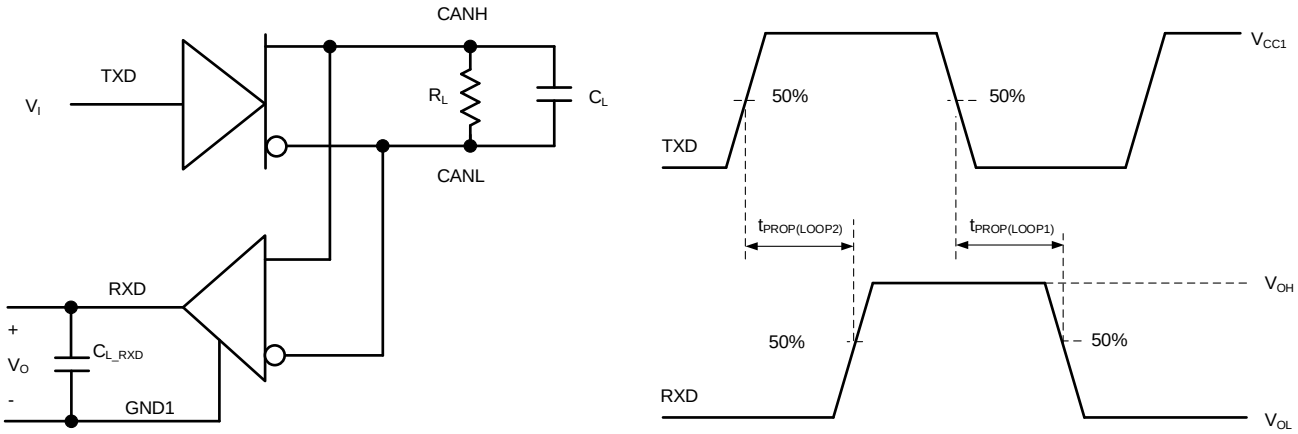


Figure 8. t_{LOOP} Test Circuit and Timing

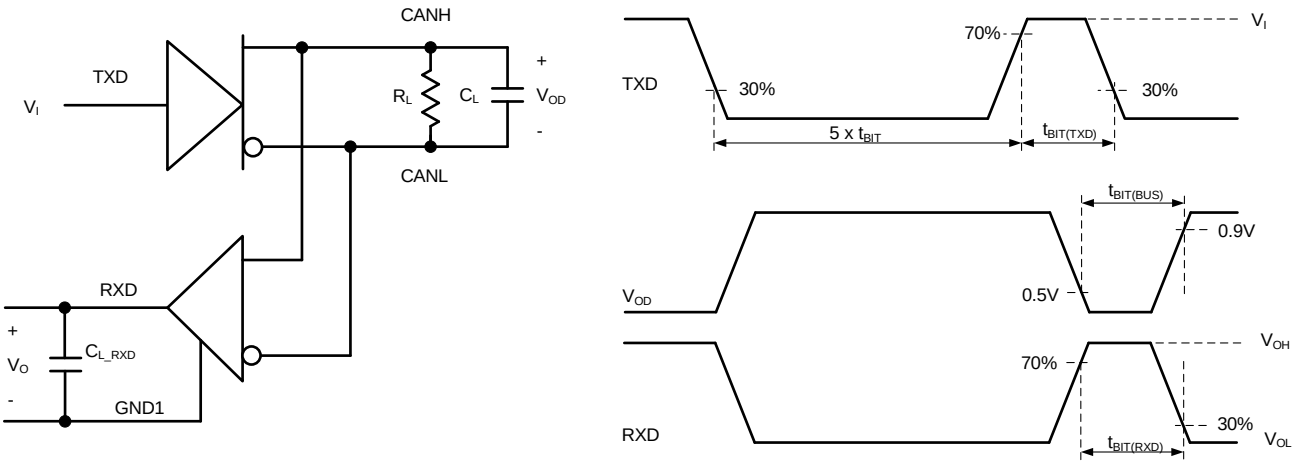


Figure 9. CAN FD Test Circuit and Timing

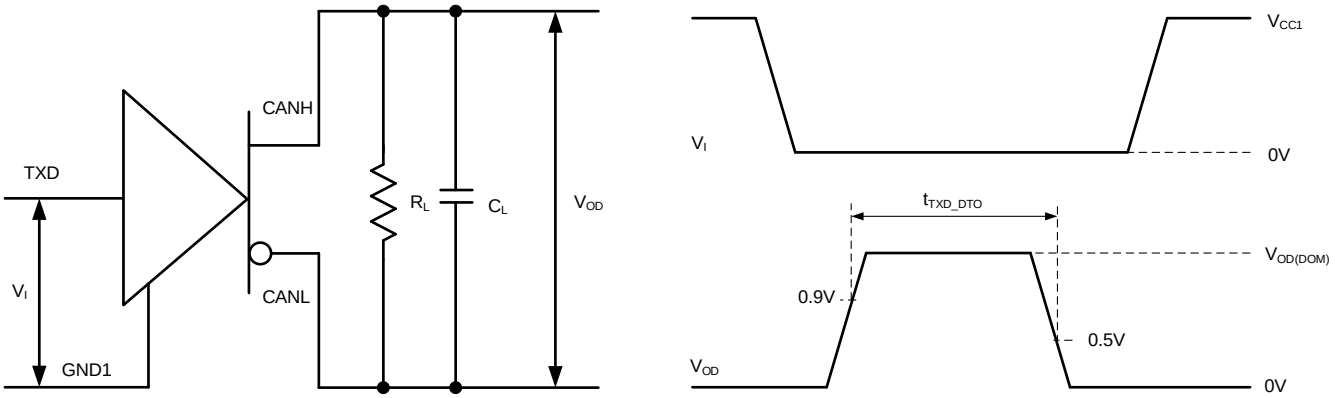


Figure 10. Dominant Time-Out Test Circuit and Timing

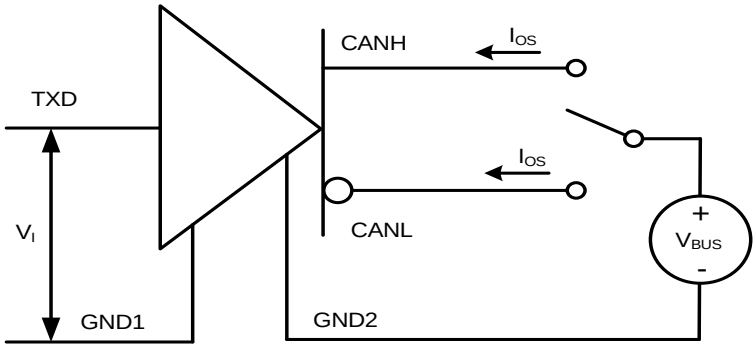


Figure 11. Driver Short Circuit Current Test Circuit

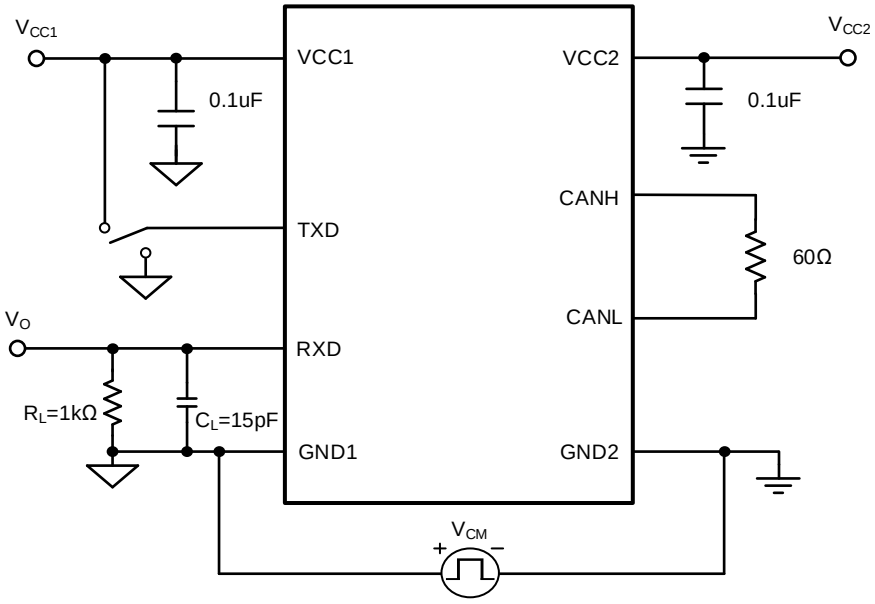


Figure 12. CMTI Test Circuit

FEATURE DESCRIPTION

The SiLM5144S is the isolated CAN transceiver that provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 5 Mbps.

CAN Bus State

The CAN bus has two logical states during operation: recessive and dominant. A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to V_{CC2} /2 via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins. A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

Normal Mode

In the normal operating mode, the CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input from the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output. The Table 1 shows the SiLM5144S function.

Table 1. TXD, RXD and Bus Function Table

Driver				Receiver		
Inputs	Outputs		BUS State	Differential Inputs	Output	BUS State
TXD	CANH	CANL		V_{ID}=CANH-CANL	RXD	
L	H	L	Dominant	$V_{ID} \geqslant V_{IT+(Max)}$	L	Dominant
H	Z	Z	Recessive	$V_{IT-(Min)} < V_{ID} < V_{IT+(Max)}$	indeterminate	indeterminate
Open	Z	Z	Recessive	$V_{ID} \leqslant V_{IT-(Min)}$	H	Recessive

TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge occurs before the timeout period expires, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal occurs on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to V_{CC2}/2 and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

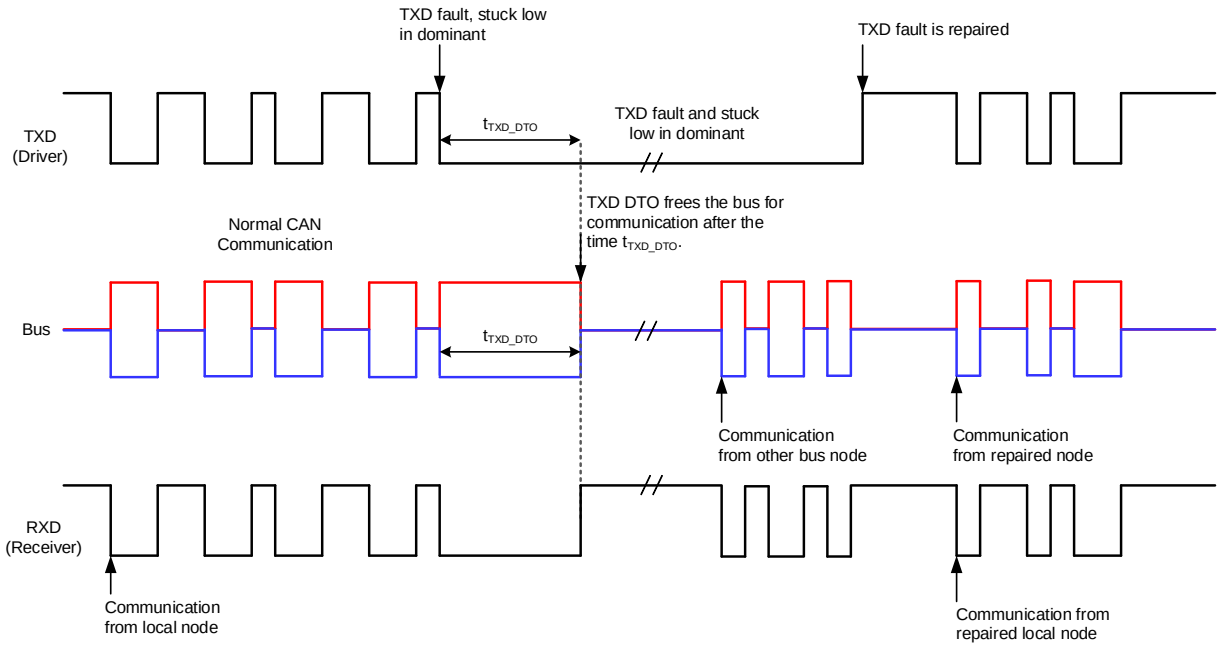


Figure 13. Example of timing diagram for TXD DTO

Under-Voltage Lockout and Default State

The supply pins have under-voltage detection which protects the bus during an under-voltage event on the V_{CC1} or V_{CC2}. If the VCC2 supply is less than 4 V (typ), the power shutdown circuits in the SiLM5144S disable the transceiver to prevent false transmissions because of an unstable supply. If the VCC1 supply is still active when this occurs, the receiver output (RXD) goes to a default HIGH (recessive) value.

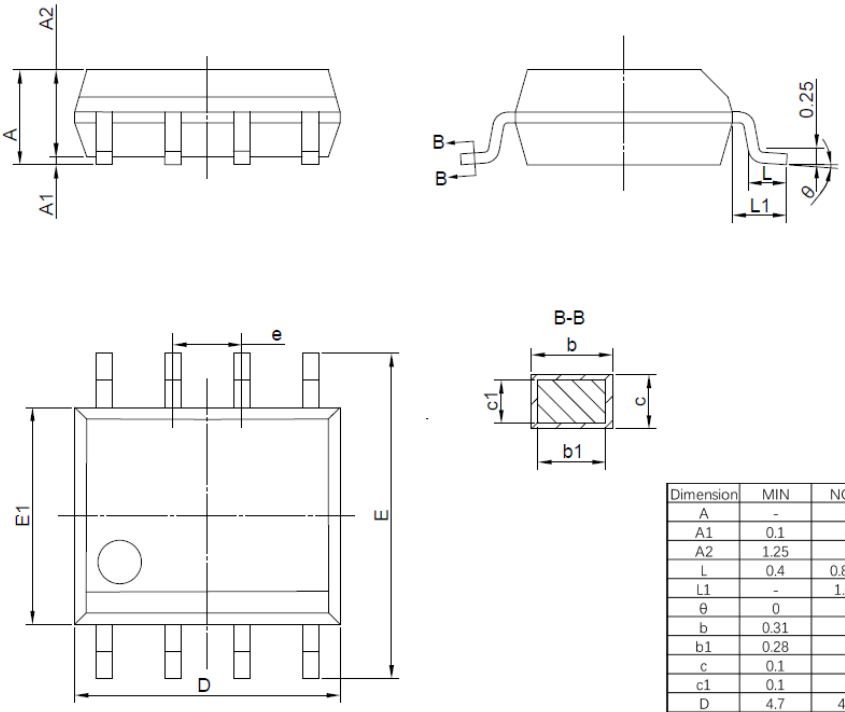
Table 2. Under-Voltage Lockout and Bus State

VCC1	VCC2	Device State	Bus Output	RXD
> UVLO	> UVLO	Functional	Pre Device State and TXD	Mirrors Bus
< UVLO	> UVLO	Protected	Recessive	Undetermined
> UVLO	< UVLO	Protected	High Impedance	Recessive (Default high)

Thermal Shutdown

If the junction temperature of the SiLM5144S exceeds the thermal shutdown threshold (T_{TSD}), the SiLM5144S turns off the CAN driver circuits, blocking the TXD-to-bus transmission path. The CAN bus are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. A hysteresis is included so that the SiLM5144S does not recover from thermal shutdown until the on-chip temperature drops below T_{TSD}-T_{TSD_HYS}.

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	4.7	4.9	5.1
E	5.8	6	6.2
E1	3.8	3.9	4
e	1.02	1.27	1.52
Unit : mm			

Figure 14. SOP8 Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2023-08-29	
Whole document	Initial datasheet release