Ultra-Compact, 1.5A Thermoelectric Cooler (TEC) Controller

GENERAL DESCRIPTION

The SLM8834 is a monolithic TEC controller with an integrated TEC controller. It has a linear power stage, a pulse-width modulation (PWM) power stage, and two zero-drift, rail-to-rail operational amplifiers.

The linear controller works with the PWM driver to control the internal power MOSFETs in an H-bridge configuration. By measuring the thermal sensor feedback voltage and using the integrated operational amplifiers as a proportional integral differential (PID) compensator to condition the signal, the SLM8834 drives current through a TEC to settle the temperature of a laser diode or a passive component attached to the TEC module to the programmed target temperature.

The SLM8834 supports negative temperature coefficient (NTC) thermistors as well as positive temperature coefficient (PTC) resistive temperature detectors (RTD). The target temperature is set as an analog voltage input either from a digital-to-analog converter (DAC) or from an external resistor divider.

The temperature control loop of the SLM8834 is stabilized by PID compensation utilizing the built in, zero drift chopper amplifiers. The internal 2.50 V reference voltage provides a 1% accurate output that is used to bias a thermistor temperature sensing bridge as well as a voltage divider network to program the maximum TEC current and voltage limits for both the heating and cooling modes. With the zero drift chopper amplifiers, extremely good long-term temperature stability is maintained via an autonomous analog temperature control loop.

FEATURES

- Integrated super low R_{DSON} MOSFETs for the TEC controller
- High efficiency single inductor architecture
- TEC voltage and current operation monitoring
- No external sense resistor required
- Independent TEC heating and cooling current limit settings
- Programmable maximum TEC voltage
- 2.0 MHz PWM driver switching frequency
- External synchronization
- Two integrated, zero drift, rail-to-rail chopper amplifiers
- Capable of NTC or RTD thermal sensors
- 2.50 V reference output with 1% accuracy
- Temperature lock indicator
- Available in a 25-ball, 2.5 mm × 2.5 mm WLCSP or in a 24-lead, 4 mm × 4 mm QFN

APPLICATIONS

- TEC temperature control
- Optical modules
- Optical fiber amplifiers
- Optical networking systems
- Instruments requiring TEC temperature control

SYSTEM BLOCK DIAGRAM

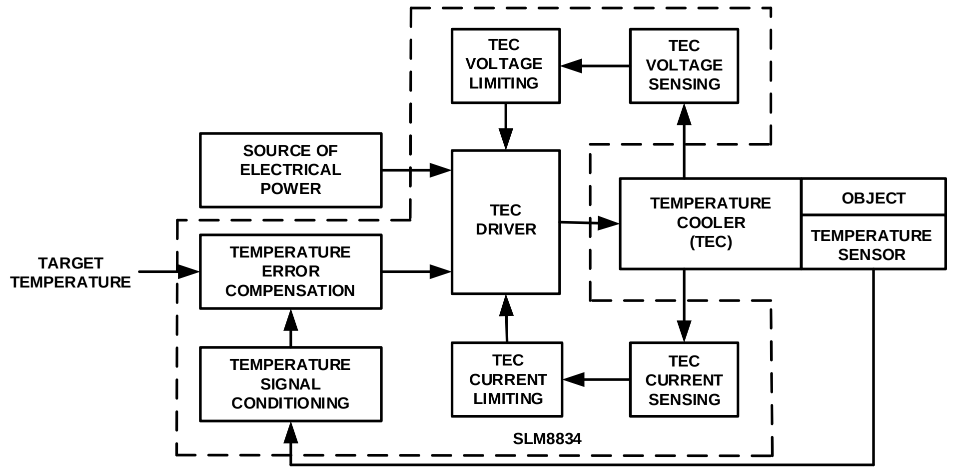


Figure 1. TEC System Block Diagram

TYPICAL APPLICATION CIRCUIT

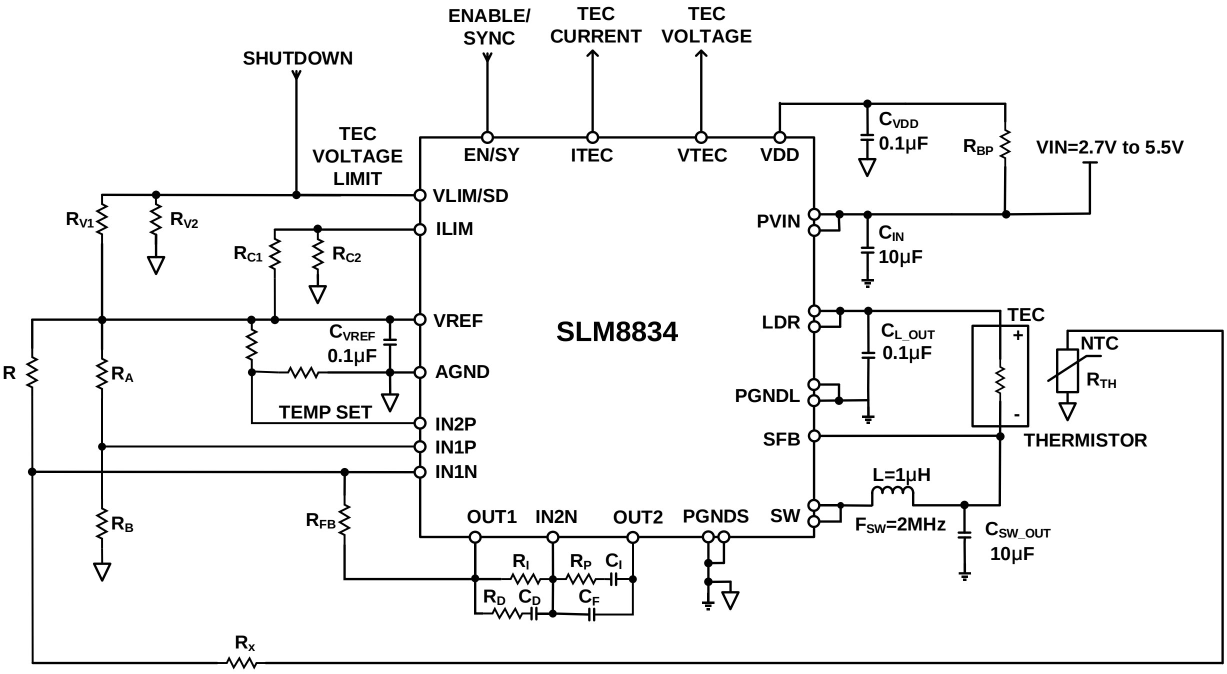


Figure 2. Typical Application Circuit with Analog PID Compensation in a Temperature Control Loop

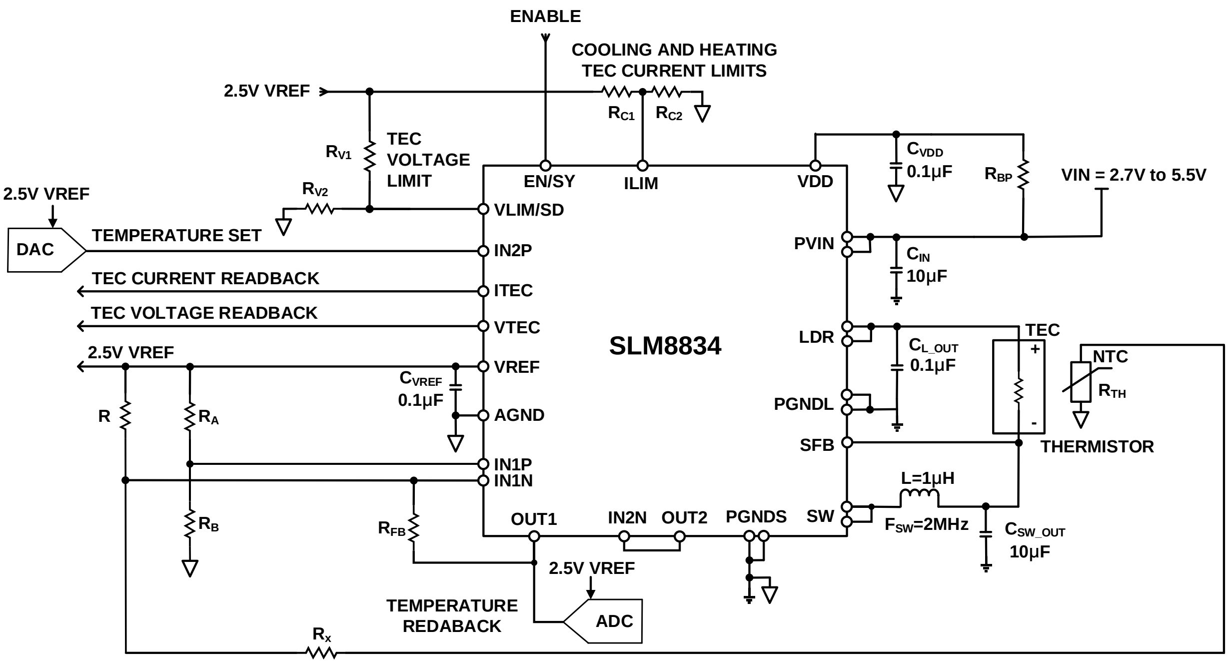
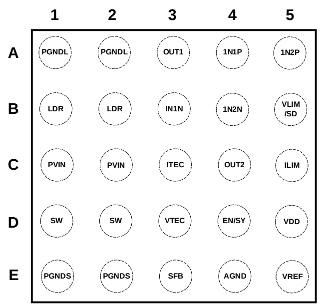
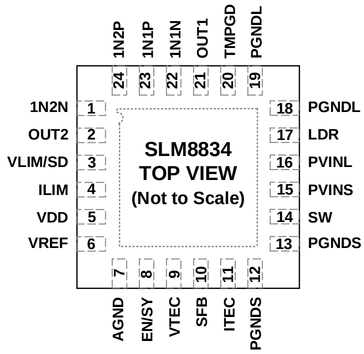


Figure 3. TEC Controller in a Digital Temperature Control Loop (WLCSP)

Table of Contents

PIN CONFIGURATION

<table>
<tr><th>Package</th><th>25-ball, 2.5 mm × 2.5 mm WLCSP</th><th>24-lead, 4 mm × 4 mm QFN</th></tr>
<tr><td>Pin Configuration (Top View)</td><td>

SLM8834
TOP VIEW
(Not to Scale)</td><td>
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PIN DESCRIPTION

Pin No.		Pin Name	Description
WLCSP	QFN		
A1, A2	18, 19	PGNDL	Power Ground of the Linear TEC Controller.
N/A[1]	20	TMPGD	Temperature Good Output.
A3	21	OUT1	Output of the Error Amplifier.
A4	23	IN1P	Noninverting Input of the Error Amplifier.
A5	24	IN2P	Noninverting Input of the Compensation Amplifier.
B1, B2	17	LDR	Output of the Linear TEC Controller.
B3	22	IN1N	Inverting Input of the Error Amplifier.
B4	1	IN2N	Inverting Input of the Compensation Amplifier.
B5	3	VLIM/SD	Voltage Limit/Shutdown. This pin sets the cooling and heating TEC voltage limits. When this pin is pulled low, the device shuts down.
C1, C2	N/A[1]	PVIN	Power Input for the TEC Controller.
N/A[1]	16	PVINL	Power Input for the Linear TEC Driver.
N/A[1]	15	PVINS	Power Input for the PWM TEC Driver.
C3	11	ITEC	TEC Current Output.
C4	2	OUT2	Output of the Compensation Amplifier.
C5	4	ILIM	Current Limit. This pin sets the TEC cooling and heating current limits.

Pin No.		Pin Name	Description
D1, D2	14	SW	Switch Node Output of the PWM TEC Controller.
D3	9	VTEC	TEC Voltage Output.
D4	8	EN/SY	Enable/Synchronization. Set this pin high to enable the device. An external synchronization clock input can be applied to this pin.
D5	5	VDD	Power for the Controller Circuits.
E1, E2	12, 13	PGNDS	Power Ground of the PWM TEC Controller.
E3	10	SFB	Feedback of the PWM TEC Controller Output.
E4	7	AGND	Signal Ground.
E5	6	VREF	2.5 V Reference Output.
N/A[1]	0	EPAD	Exposed Pad. Solder to the analog ground plane on the board.

N/A[1]: Not Available.

ORDERING INFORMATION

Order Part No.	Package	QTY
SLM8834FA-7G	25-ball, 2.5 mm × 2.5 mm WLCSP	3000/Reel
SLM8834EC	24-lead, 4 mm × 4 mm QFN	1000/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Unit
V_{PVIN}	PVIN to PGNDL / PGNDS (WLCSP)	-0.3	6.0	V
V_{PVINL}, V_{PVINS}	PVINL to PGNDL; PVINS to PGNDS (QFN)	-0.3	6.0	V
V_{LDR}	LDR to PGNDL (WLCSP)	-0.3	V_{PVIN}	V
	LDR to PGNDL (QFN)	-0.3	V_{PVINL}	V
V_{SW}	SW to PGNDS	-0.3	6.0	V
V_{SFB}, V_{SW}	SFB / VLIM/SD / IN1P / IN1N / IN2P / IN2N / EN/SY to AGND	-0.3	V_{VDD}	V
V_{GND}	AGND to PGNDL / PGNDS	-0.3	0.3	V
V_{VDD}, V_{ITEC},	VDD / OUT1 / OUT2 /ITEC / VTEC to AGND	-0.3	6.0	V
V_{VREF}	VREF to AGND	-0.3	3.0	V
I_{VREF}	VREF Current		20	mA
I_{OUT1}	OUT1 to AGND		50	mA
I_{OUT2}	OUT2 to AGND		50	mA
I_{ITEC}	ITEC Current		50	mA
I_{VTEC}	VTEC Current		50	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C

Note:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATION CONDITIONS

Symbol	Description	Min	Max	Unit
V_{PVIN}	Driver supply voltage range (WLCSP)	2.7	5.5	V
V_{PVINL}, V_{PVINS}	Driver supply voltage range (QFN)	2.7	5.5	V
V_{VDD}	Controller Supply Voltage	2.7	5.5	V
T_J	Operation junction temperature	-40	125	°C

QUALIFICATION RATINGS

Symbol	Description	Value	Unit
V_{ESD}	HBM	2000	V
	MM	200	V
	CDM	1500	V
I_{LU}	Latch-up	100	mA

THERMAL INFORMATION

Symbol	Description	Value	Unit
R_{TH-JA}	Junction to Ambient (WLCSP)	48	°C/W
	Junction to Ambient (QFN)	37	°C/W
R_{TH-JC}	Junction to Case (WLCSP)	0.6	°C/W
	Junction to Case (QFN)	1.65	°C/W

ELECTRICAL CHARACTERISTICS

Test condition is V_{PVIN} = V_{VDD} =5V, V_{PVINL} = V_{PVINS} = V_{VDD} =5V, T_J = −40°C ~ +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supply						
I_{VDD}	Supply Current	PWM switching		12		mA
I_{SD}	Shutdown Current	EN/SY = AGND or VLIM/SD = AGND		350	700	μA
UVLO	Under Voltage Lockout Threshold	V_{VDD} Rising	2.45	2.55	2.65	V
	Under Voltage Lockout Hysteresis		80	90	100	mV
Reference Voltage						
V_{VREF}	Reference Voltage	I_{VREF} = 0 mA to 10 mA	2.475	2.50	2.525	V
Linear Output						
V_{LDR}	Output Voltage Low	I_{LDR} = 0 A		0		V
	Output Voltage High			V_{PVIN}		
I_{LDR_SOURCE}	Maximum Source Current	T_J = -40°C to +105°C	1.5			A
		T_J = -40°C to +125°C	1.2			
I_{LDR_SINK}	Maximum Sink Current	T_J = -40°C to +105°C			1.5	A
		T_J = -40°C to +125°C			1.2	
R_{DSON_PMOS}	P-MOSFET ON Resistance (I_{LDR} = 0.6 A)	WLCSP, V_{PVIN} = 5.0 V		35	50	mΩ
		WLCSP, V_{PVIN} = 3.3 V		42	57	
		QFN, V_{PVIN} = 5.0 V		50	65	
		QFN, V_{PVIN} = 3.3 V		53	70	
R_{DSON_NMOS}	N-MOSFET ON Resistance (I_{LDR} = 0.6 A)	WLCSP, V_{PVIN} = 5.0 V		27	40	mΩ
		WLCSP, V_{PVIN} = 3.3 V		32	45	
		QFN, V_{PVIN} = 5.0 V		37	55	
		QFN, V_{PVIN} = 3.3 V		40	65	
$I_{LDR\_P\_LKG}$	P-MOSFET Leakage Current			0.1	10	μA
$I_{LDR\_N\_LKG}$	N-MOSFET Leakage Current			0.1	10	μA
ALDR	Linear Amplifier Gain			40		V/V
$I_{LDR\_SH\_GNDL}$	LDR Short-Circuit Threshold	LDR short to PGNDL, enter hiccup		2.2		A
$I_{LDR\_SH\_PVIN(L)}$	LDR Short-Circuit Threshold	LDR short to PVIN, enter hiccup		-2.2		A
T_{HICCUP}	Hiccup Cycle			15		ms
PWM Output						
V_{SFB}	Output Voltage Low	I_{SFB} = 0 A		0.06 x V_{PVIN}		V
	Output Voltage High			0.93 x V_{PVIN}		
I_{SW_SOURCE}	Maximum Source Current	T_J = -40°C to +105°C	1.5			A

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
		T_J = -40°C to +125°C	1.2			
I_{SW_SINK}	Maximum Sink Current	T_J = -40°C to +105°C			1.5	A
		T_J = -40°C to +125°C			1.2	
R_{DSON_PMOS}	P-MOSFET ON Resistance (I_{LDR} = 0.6 A)	WLCSP, V_{PVIN} = 5.0 V		47	65	mΩ
		WLCSP, V_{PVIN} = 3.3 V		60	80	
		QFN, V_{PVIN} = 5.0 V		60	80	
		QFN, V_{PVIN} = 3.3 V		70	95	
R_{DSON_NMOS}	N-MOSFET ON Resistance (I_{LDR} = 0.6 A)	WLCSP, V_{PVIN} = 5.0 V		40	60	mΩ
		WLCSP, V_{PVIN} = 3.3 V		45	65	
		QFN, V_{PVIN} = 5.0 V		45	75	
		QFN, V_{PVIN} = 3.3 V		55	85	
$I_{SW\_P\_LKG}$	P-MOSFET Leakage Current			0.1	10	µA
$I_{SW\_N\_LKG}$	N-MOSFET Leakage Current			0.1	10	µA
t_{SW_R}	SW Node Rise Time	C_{SW} = 1 nF		1		ns
D_{SW}	PWM Duty Cycle		6		93	%
I_{SFB}	SFB Input Bias Current			1	2	µA
PWM Oscillator						
f_{OSC}	Internal Oscillator Frequency	EN/SY high	1.85	2.0	2.15	MHz
V_{EN/SY_ILOW}	EN/SY Input Voltage Low				0.8	V
V_{EN/SY_IHIGH}	EN/SY Input Voltage High		2.1			V
f_{SYNC}	External Synchronization Frequency		1.85		3.25	MHz
D_{SYNC}	Synchronization Pulse Duty Cycle		10		90	%
t_{SYNC_PWM}	EN/SY Rising to PWM Rising Delay			50		ns
t_{SY_LOCK}	EN/SY to PWM Lock Time	Number of SYNC cycles			10	Cycles
$I_{EN/SY}$	EN/SY Input Current			0.3	0.5	µA
$I_{PULL\text{-}DOWN}$	Pull-Down Current			0.3	0.5	µA
Error/Compensation Amplifiers						
V_{OS1}	Input Offset Voltage	V_{CM1} = 1.5 V, V_{OS1} = V_{IN1P} – V_{IN1N}		10	100	µV
V_{OS2}	Input Offset Voltage	V_{CM1} = 1.5 V, V_{OS2} = V_{IN2P} – V_{IN2N}		10	100	µV
V_{CM1}, V_{CM2}	Input Voltage Range		0		V_{VDD}	V
$CMRR_1$, CMR_2	Common-Mode Rejection Ratio (CMRR)	V_{CM1}, V_{CM2} = 0.2 V to V_{VDD} – 0.2 V		120		dB
V_{OH1}, V_{OH2}	Output Voltage High		V_{VDD} – 0.4			V
V_{OL1}, V_{OL2}	Output Voltage Low				10	mV
$PSRR_1$, $PSRR_2$	Power Supply Rejection Ratio (PSRR)			120		dB

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{OUT1}, I_{OUT2}	Output Current	Sourcing and sinking	5			mA
GBW_1, GBW_2	Gain Bandwidth Product	VOUT1, VOUT2 = 0.5 V to VVDD – 1 V		2		MHz
TEC Current Limit						
V_{ILIMC}	ILIM Input Voltage Range Cooling		1.3		V_{VREF} – 0.2	V
V_{ILIMH}	ILIM Input Voltage Range Heating		0.2		1.2	V
V_{ILIMC_TH}	Current-Limit Threshold Cooling	V_{ITEC} = 0.5 V	1.98	2.0	2.02	V
V_{ILIMH_TH}	Current-Limit Threshold Heating	V_{ITEC} = 2 V	0.48	0.5	0.52	V
I_{ILIMH}	ILIM Input Current Heating		-0.2		+0.2	µA
I_{ILIMC}	ILIM Input Current Cooling	Sourcing current	37.5	40	42.5	µA
$I_{COOL\_HEAT\_TH}$	Cooling to Heating Current Detection Threshold			40		mA
TEC Voltage Limit						
A_{VLIM}	Voltage Limit Gain	$(V_{DRL} - V_{SFB})/V_{VLIM}$		2		V/V
V_{LIM}	VLIM/SD Input Voltage Range		0.2		$V_{VDD}/2$	V
I_{ILIMC}	VLIM/SD Input Current Cooling	$V_{OUT2} < V_{VREF}/2$	-0.2		+0.2	µA
I_{ILIMH}	VLIM/SD Input Current Heating	$V_{OUT2} > V_{VREF}/2$, sinking current	8	10	12	µA
TEC Current Measurement (WLCSP)						
R_{CS}	Current Sense Gain	V_{PVIN} = 3.3 V		0.525		V/A
		V_{PVIN} = 5 V		0.525		V/A
I_{LDR_ERROR}	Current Measurement Accuracy	700mA ≤ I_{LDR}≤ 1 A, V_{PVIN} = 3.3 V	-10		+10	%
		800mA ≤ I_{LDR}≤ 1 A, V_{PVIN} = 5 V	-10		+10	%
$V_{ITEC\_@\_700mA}$	ITEC Voltage Accuracy	V_{PVIN} = 3.3 V, cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.597	1.618	1.649	V
$V_{ITEC\_@\_-700mA}$		V_{PVIN} = 3.3 V, heating, $V_{VREF}/2 - I_{LDR} \times R_{CS}$	0.846	0.883	0.891	V
$V_{ITEC\_@\_800mA}$		V_{PVIN} = 5 V, cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.657	1.678	1.718	V
$V_{ITEC\_@\_-800mA}$		V_{PVIN} = 5 V, heating, $V_{VREF}/2 - I_{LDR} \times R_{CS}$	0.783	0.822	0.836	V
TEC Current Measurement (QFN)						
R_{CS}	Current Sense Gain	V_{PVIN} = 3.3 V		0.525		V/A
		V_{PVIN} = 5 V		0.525		V/A
I_{LDR_ERROR}	Current Measurement Accuracy	700mA ≤ I_{LDR}≤ 1 A, V_{PVIN} = 3.3 V	-15		+15	%
		800mA ≤ I_{LDR}≤ 1 A, V_{PVIN} = 5 V	-15		+15	%
$V_{ITEC\_@\_700mA}$	ITEC Voltage Accuracy	V_{PVIN} = 3.3 V, cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.374	1.618	1.861	V
$V_{ITEC\_@\_-700mA}$		V_{PVIN} = 3.3 V, heating, $V_{VREF}/2 - I_{LDR} \times R_{CS}$	0.750	0.883	1.015	V
$V_{ITEC\_@\_800mA}$		V_{PVIN} = 5 V, cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.419	1.678	1.921	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{ITEC\_@\_-800mA}$		V_{PVIN} = 5 V, heating, $V_{VREF}/2 - I_{LDR} \times R_{CS}$	0.705	0.830	0.955	V
V_{ITEC}	ITEC Voltage Output Range	I_{TEC} = 0 A	0		V_{VREF} – 0.05	V
V_{ITEC_BIAS}	ITEC Bias Voltage	I_{LDR} = 0 A	1.215	1.250	1.285	V
I_{ITEC_Max}	Maximum ITEC Output Current		-2		+2	mA
TEC Voltage Measurement						
A_{VTEC}	Voltage Sense Gain		0.24	0.25	0.26	V/V
$V_{VTEC\_@\_1\_V}$	Voltage Measurement Accuracy	$V_{LDR} - V_{SFB}$ = 1 V, $V_{VREF}/2 + A_{VTEC} \times (V_{LDR} - V_{SFB})$	1.475	1.500	1.525	V
V_{VTEC}	VTEC Output Voltage Range		0.005		2.625	V
V_{VTEC_B}	VTEC Bias Voltage	$V_{LDR} = V_{SFB}$	1.225	1.250	1.275	V
I_{VTEC_Max}	Maximum VTEC Output Current		-2		+2	mA
Temperature Good (QFN Only)						
V_{TMPGD_LO}	TMPGD Low Output Voltage	No load			0.4	V
V_{TMPGD_HO}	TMPGD High Output Voltage	No load	2.0			V
R_{TMPGD_LOW}	TMPGD Output Low Impedance			25		Ω
R_{TMPGD_HIGH}	TMPGD Output High Impedance			25		Ω
V_{OUT1_THH}	High Threshold	IN2N tied to OUT2, V_{IN2P} = 1.5 V		1.54	1.56	V
V_{OUT1_THL}	Low Threshold	IN2N tied to OUT2, V_{IN2P} = 1.5 V	1.44	1.46		V
Internal Soft Start						
tSS	Soft Start Time			80		ms
VLIM/SD SHUTDOWN						
V_{VLIM/SD_THL}	VLIM/SD Low Voltage Threshold				0.07	V
Thermal SHUTDOWN						
T_{SHDN_TH}	Thermal Shutdown Threshold			170		°C
T_{SHDN_HYS}	Thermal Shutdown Hysteresis			17		°C

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

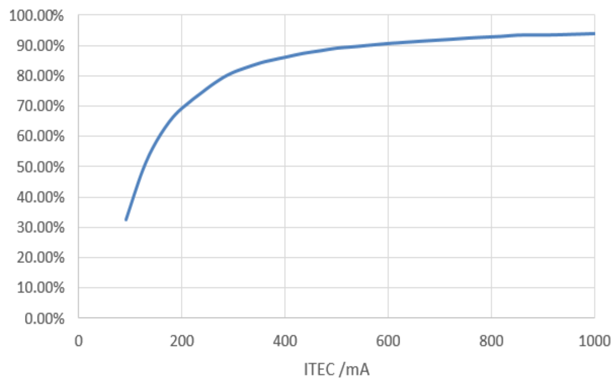


Figure 4. Efficiency vs. ITEC at V_{IN}=3.3V in Cooling Mode

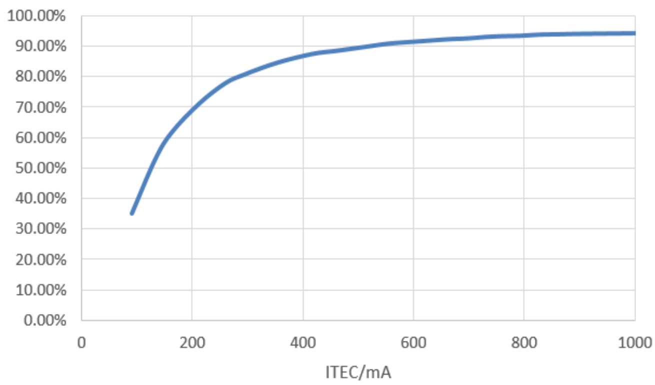


Figure 5. Efficiency vs. ITEC at V_{IN}=3.3V in Heating Mode

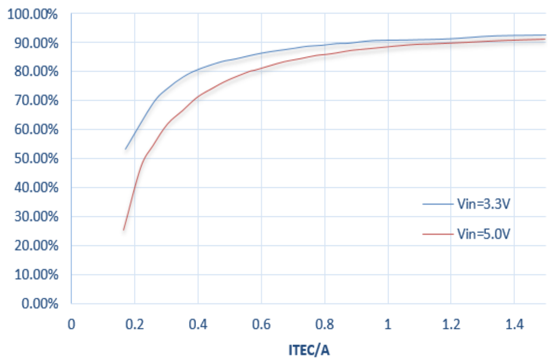


Figure 6. Efficiency vs. ITEC at V_{IN}=3.3V and 5.0V with 2Ω Load in Cooling Mode

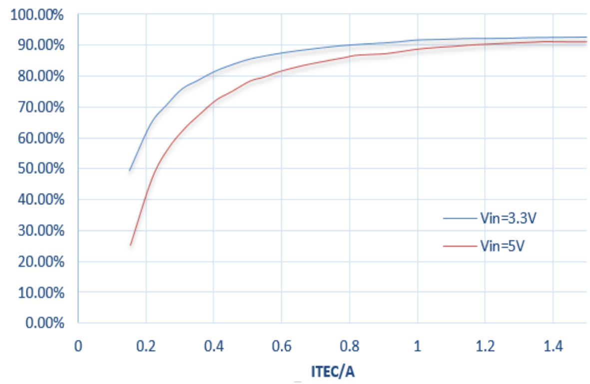


Figure 7. Efficiency vs. ITEC at V_{IN}=3.3V and 5.0V with 2Ω Load in Heating Mode

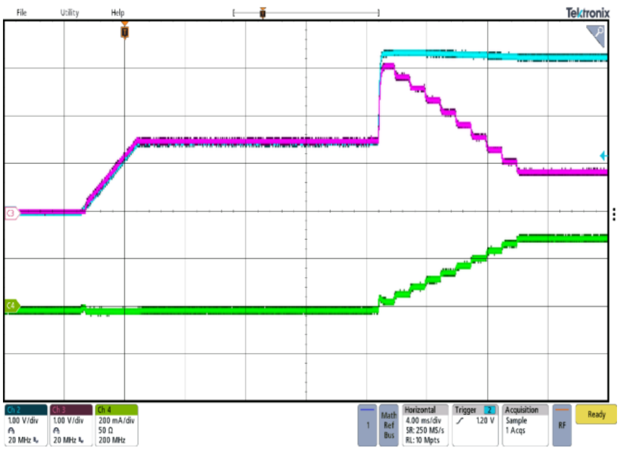


Figure 8. Soft Start into Cooling Mode
(V_{IN}=3.3V with 5Ω load)
CH2: LDR (TEC+), CH3: SFB (TEC-), CH4: ITEC

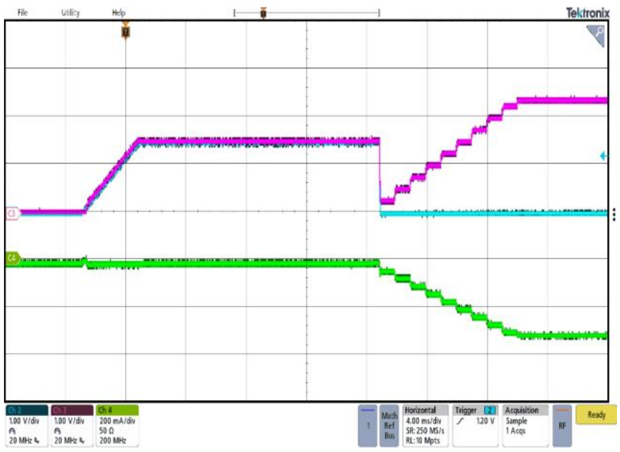


Figure 9. Soft Start into Heating Mode
(V_{IN}=3.3V with 5Ω load)
CH2: LDR (TEC+), CH3: SFB (TEC-), CH4: ITEC

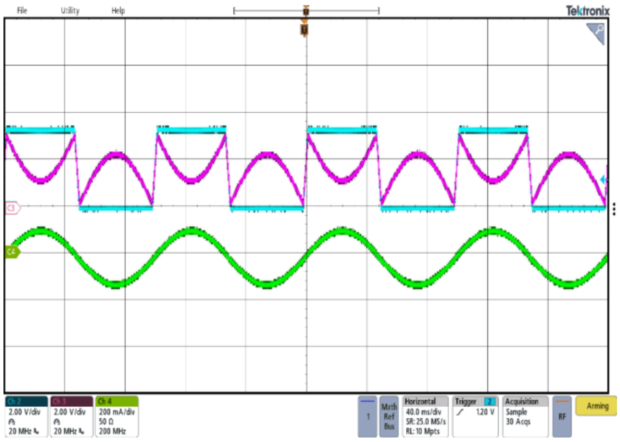


Figure 10. Cooling to Heating Transient
CH2: LDR (TEC+), CH3: SFB (TEC-), CH4: ITEC

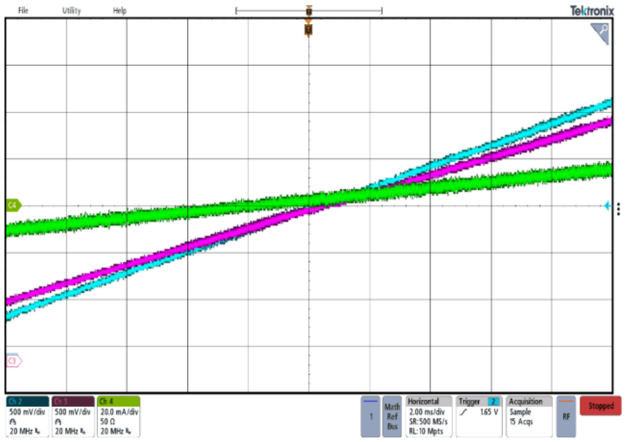


Figure 11. Zero Acrossing TEC Current Zoom-in from Heating to Cooling
CH2: LDR (TEC+), CH3: SFB (TEC-), CH4: ITEC

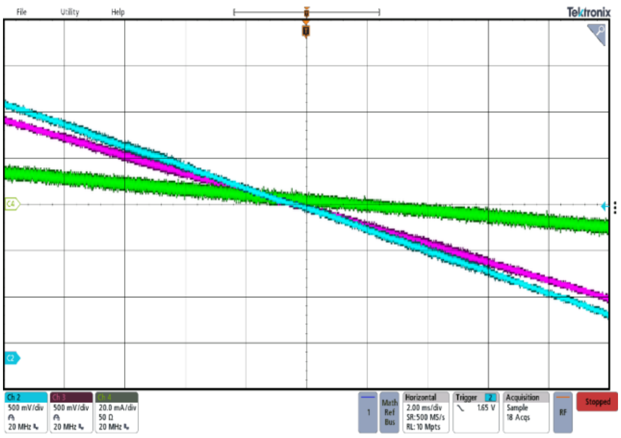


Figure 12. Zero Acrossing TEC Current Zoom-in from Cooling to Heating
CH2: LDR (TEC+), CH3: SFB (TEC-), CH4: ITEC

APPLICATION INFORMATION

The SLM8834 is a single chip TEC controller that sets and stabilizes a TEC temperature. A voltage applied to the input of the SLM8834 corresponds to the temperature setpoint of the target object attached to the TEC. The SLM8834 controls an internal FET H-bridge whereby the direction of the current fed through the TEC can be either positive (for cooling mode), to pump heat away from the object attached to the TEC, or negative (for heating mode), to pump heat into the object attached to the TEC. Temperature is measured with a thermal sensor attached to the target object and the sensed temperature (voltage) is fed back to the SLM8834 to complete a closed thermal control loop of the TEC. For the best overall stability, couple the thermal sensor close to the TEC. In most laser diode modules, a TEC and a NTC thermistor are already mounted in the same package to regulate the laser diode temperature.

The TEC is differentially driven in an H-bridge configuration. The SLM8834 drives its internal MOSFET transistors to provide the TEC current. To provide good power efficiency and zero crossing quality, only one side of the H-bridge uses a PWM driver. Only one inductor and one capacitor are required to filter out the switching frequency. The other side of the H-bridge uses a linear output without requiring any additional circuitry. This proprietary configuration allows the SLM8834 to provide efficiency of >90%. For most applications, a 1 µH inductor, a 10 µF capacitor, and a switching frequency of 2 MHz maintain less than 1% of the worst-case output voltage ripple across a TEC.

The maximum voltage across the TEC and the current flowing through the TEC are set by using the VLIM/SD and ILIM pins. The maximum cooling and heating currents can be set independently to allow asymmetric heating and cooling limits. For additional details, see the Maximum TEC Voltage Limit section and the Maximum TEC Current Limit section.

ANALOG PID CONTROL

The SLM8834 integrates two self-correcting, auto-zeroing amplifiers (Chopper 1 and Chopper 2). The Chopper 1 amplifier takes a thermal sensor input and converts or regulates the input to a linear voltage output. The OUT1 voltage is proportional to the object temperature. The OUT1 voltage is fed into the compensation amplifier (Chopper 2) and is compared with a temperature setpoint voltage, which creates an error voltage that is proportional to the difference. For autonomous analog temperature control, Chopper 2 can be used to implement a PID network as shown in Figure 2 to set the overall stability and response of the thermal loop. Adjusting the PID network optimizes the step response of the TEC control loop. A compromised settling time and the maximum current ringing become available when this adjustment is done.

DIGITAL PID CONTROL

The SLM8834 can also be configured for use in a software controlled PID loop. In this scenario, the Chopper 1 amplifier can either be left unused or configured as a thermistor input amplifier connected to an external temperature measurement analog-to-digital converter (ADC). If Chopper 1 is left unused, tie IN1N and IN1P to AGND. The Chopper 2 amplifier is used as a buffer for the external DAC, which controls the temperature setpoint. Connect the DAC to IN2P and short the IN2N and OUT2 pins together. See Figure 3 for an overview of how to configure the SLM8834 external circuitry for digital PID control.

POWERING THE CONTROLLER

The SLM8834 operates at an input voltage range of 2.7 V to 5.5 V that is applied to the VDD pin and the PVIN pin for the WLCSP (the PVINS pin and PVINL pin for the LFCSP). The VDD pin is the input power for the driver and internal reference. The PVIN input power pins are combined for both the linear and the switching driver. Apply the same input voltage to all power input pins: VDD and PVIN. In some circumstances, an RC lowpass filter can be added optionally between the PVIN for the WLCSP (PVINS and PVINL for the LFCSP) and VDD pins to prevent high frequency noise from entering VDD, as shown in Figure 3. The capacitor and resistor values are typically 10 Ω and 100 nF, respectively. When configuring power supply to the SLM8834, keep in mind that at high current loads, the input voltage may drop substantially due to a voltage drop on the wires between the front-end power supply and the PVIN for the WLCSP (PVINS and PVINL for the LFCSP) pin. Leave a proper voltage margin when designing the front-end power supply to maintain the performance. Minimize the trace length from the power supply to the PVIN for the WLCSP (PVINS and PVINL for the LFCSP) pin to help mitigate the voltage drop.

ENABLE AND SHUTDOWN

To enable the SLM8834, apply a logic high voltage to the EN/SY pin while the voltage at the VLIM/SD pin is above the maximum shutdown threshold of 0.07 V. If either the EN/SY pin voltage is set to logic low or the VLIM/SD voltage is below 0.07 V, the controller goes into an ultralow current state. The current drawn in shutdown mode is 350 µA typically. Most of the current is consumed by the VREF circuit block, which is always on even when the device is disabled or shut down. The device can also be enabled when an external synchronization clock signal is applied to the EN/SY pin, and the voltage at VLIM/SD input is above 0.07 V. Table 1 shows the combinations of the two input signals that are required to enable the SLM8834.

Table 1. Enable Pin Combinations

EN/SY Input		VLIM/SD Input	Controller
>2.1 V		>0.07 V	Enabled
Switching between high >2.1 V and low < 0.8 V		>0.07 V	Enabled
<0.8 V		No effect[1]	Shutdown
Floating		No effect[1]	Shutdown
No effect[1]		≤0.07 V	Shutdown

[1] No effect means this signal has no effect in shutting down or in enabling the device.

OSCILLATOR CLOCK FREQUENCY

The SLM8834 has an internal oscillator that generates a 2.0 MHz switching frequency for the PWM output stage. This oscillator is active when the enabled voltage at the EN/SY pin is set to a logic level higher than 2.1 V and the VLIM/SD pin voltage is greater than the shutdown threshold of 0.07 V.

EXTERNAL CLOCK OPERATION

The PWM switching frequency of the SLM8834 can be synchronized to an external clock from 1.85 MHz to 3.25 MHz, applied to the EN/SY input pin as shown on Figure 13.

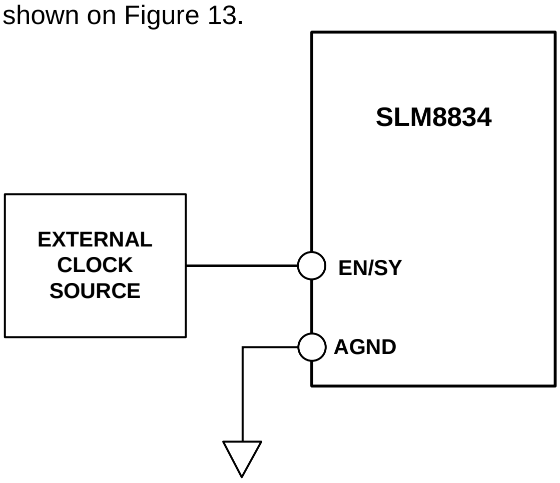


Figure 13. Synchronize to an External Clock

CONNECTING MULTIPLE SLM8834 DEVICES

Multiple SLM8834 devices can be driven from a single master clock signal by connecting the external clock source to the EN/SY pin of each slave device. The input ripple can be greatly reduced by operating the SLM8834 devices 180° out of phase from each other by placing an inverter at one of the EN/SY pins, as shown in Figure 14.

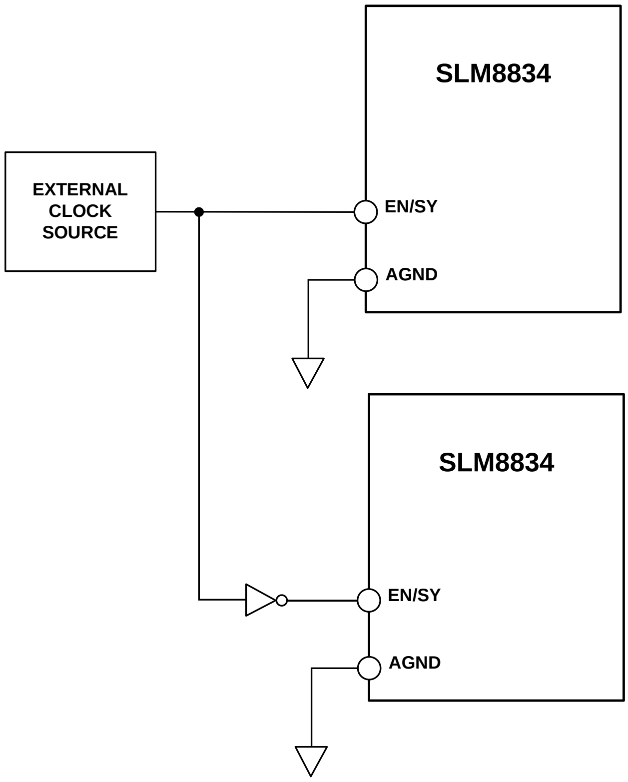


Figure 14. Multiple SLM8834 Devices Driven from a Master Clock

TEMPERATURE LOCK INDICATOR (LFCSP ONLY)

The TMPGD outputs logic high when the temperature error amplifier output voltage, V_{OUT1}, reaches the IN2P temperature setpoint (TEMPSET) voltage. The TMPGD has a detection range between 1.46 V and 1.54 V of V_{OUT1} and hysteresis. The TMPGD function allows direct interfacing either to the microcontrollers or to the supervisory circuitry.

SOFT START ON POWER-UP

The SLM8834 has an internal soft start circuit that generates a ramp with a typical 80 ms profile to minimize inrush current during power-up. The settling time and the final voltage across the TEC depends on the TEC voltage required by the control voltage of voltage loop. The higher the TEC voltage is, the longer it requires to be built up.

When the SLM8834 is first powered up, the linear side discharges the output of any prebias voltage. As soon as the prebias is eliminated, the soft start cycle begins. During the soft start cycle, both the PWM and linear outputs track the internal soft start ramp until they reach midscale, where the control voltage, V_C, is equal to the bias voltage, V_B. From the midscale voltage, the PWM and linear outputs are then controlled by V_C and diverge from each other until the required differential voltage is developed across the TEC or the differential voltage reaches the voltage limit. The voltage developed across the TEC depends on the control point at that moment in time. Figure 15 shows an example of the soft start in cooling mode. Note that, as both the LDR and SFB voltages increase with the soft start ramp and approach V_B, the ramp slows down to avoid possible current overshoot at the point where the TEC voltage starts to build up.

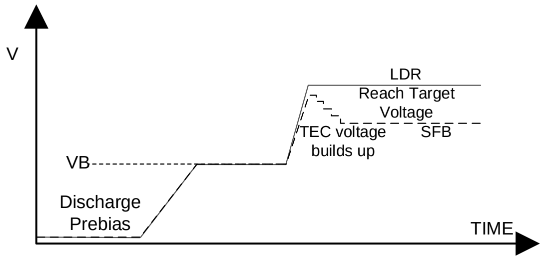


Figure 15. Soft Start Profile in Cooling Mode

TEC VOLTAGE/CURRENT MONITOR

The TEC real-time voltage and current are detectable at VTEC and ITEC, respectively.

VOLTAGE MONITOR

VTEC is an analog voltage output pin with a voltage proportional to the actual voltage across the TEC. A center VTEC voltage of 1.25 V corresponds to 0 V across the TEC. Convert the voltage at VTEC and the voltage across the TEC using the following equation:

$V_{VTEC} = 1.25\ V + 0.25 \times (V_{LDR} - V_{SFB})$

CURRENT MONITOR

ITEC is an analog voltage output pin with a voltage proportional to the actual current through the TEC. A center ITEC voltage of 1.25 V corresponds to 0 A through the TEC. Convert the voltage at ITEC and the current through the TEC using the following equations:

$V_{ITEC\_COOLING} = 1.25\ V + I_{LDR} \times R_{CS}$

where the current sense gain (R_{CS}) is 0.525 V/A.

$V_{ITEC\_HEATING} = 1.25\ V - I_{LDR} \times R_{CS}$

MAXIMUM TEC VOLTAGE LIMIT

The maximum TEC voltage is set by applying a voltage divider at the VLIM/SD pin to protect the TEC. The voltage limiter operates bidirectionally and allows the cooling limit to be different from the heating limit.

USING A RESISTOR DIVIDER TO SET THE TEC VOLTAGE LIMIT

Separate voltage limits are set using a resistor divider. The internal current sink circuitry connected to VLIM/SD draws a current when the SLM8834 drives the TEC in a heating direction, which lowers the voltage at VLIM/SD. The current sink is not active when the TEC is driven in a cooling direction; therefore, the TEC heating voltage limit is always lower than the cooling voltage limit.

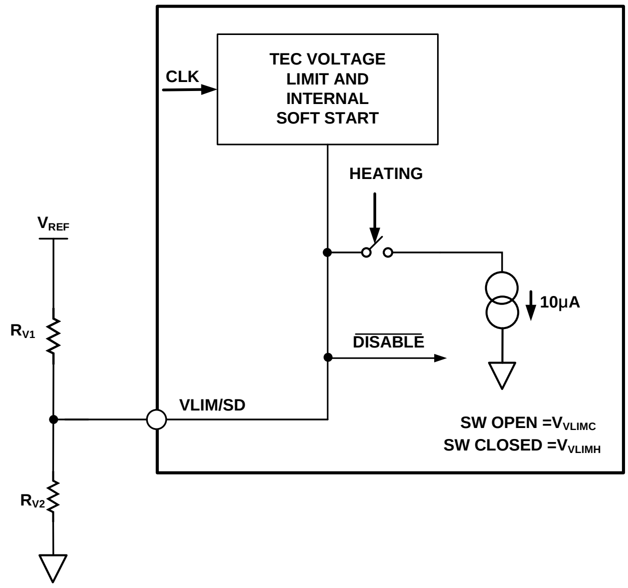


Figure 16. Using a Resistor Divider to Set the TEC Voltage Limit

Calculate the cooling and heating limits using the following equations:

$V_{VLIM\_COOLING} = V_{REF} \times R_{V2}/(R_{V1} + R_{V2})$

where V_{REF} = 2.5 V.

$V_{VLIM\_HEATING} = V_{VLIM\_COOLING} - I_{SINK\_VLIM} \times R_{V1}||R_{V2}$

where I_{SINK_VLIM} = 10 μA.

$V_{TEC\_MAX\_COOLING} = V_{VLIM\_COOLING} \times A_{VLIM}$

where A_{VLIM} = 2 V/V.

$V_{TEC\_MAX\_HEATING} = V_{VLIM\_HEATING} \times A_{VLIM}$

MAXIMUM TEC CURRENT LIMIT

To protect the TEC, separate maximum TEC current limits in cooling and heating directions are set by applying a voltage combination at the ILIM pin.

USING A RESISTOR DIVIDER TO SET THE TEC CURRENT LIMIT

The internal current sink circuitry connected to ILIM draws a 40 μA current when the SLM8834 drives the TEC in a cooling direction, which allows a high cooling current. Use the following equations to calculate the maximum TEC currents:

$V_{ILIM\_HEATING} = V_{REF} \times R_{C2}/(R_{C1} + R_{C2})$

where V_{REF} = 2.5 V.

$V_{ILIM\_COOLING} = V_{ILIM\_HEATING} + I_{SINK\_ILIM} \times R_{C1}||R_{C2}$

where I_{SINK_ILIM} = 40 μA.

$$I_{TEC\_MAX\_COOLING} = \frac{V_{ILIM\_COOLING} - 1.25\ V}{R_{CS}}$$

where R_{CS} = 0.525 V/A.

$$I_{TEC\_MAX\_HEATING} = \frac{1.25\ \text{V} - V_{ILIM\_HEATING}}{R_{CS}}$$

$V_{ILIM\_HEATING}$ must not exceed 1.2 V and $V_{ILIM\_COOLING}$ must be more than 1.3 V to leave proper margins between the heating and the cooling modes.

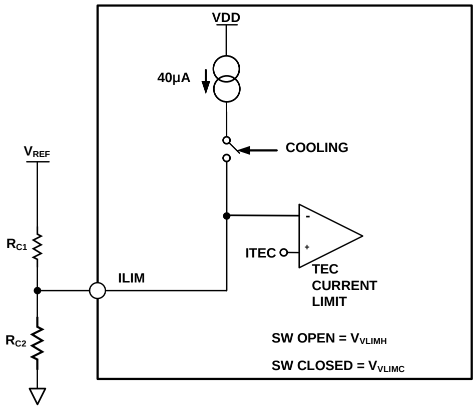


Figure 17. Using a Resistor Divider to Set the TEC Current Limit

CLASSIFICATION REFLOW PROFILS

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

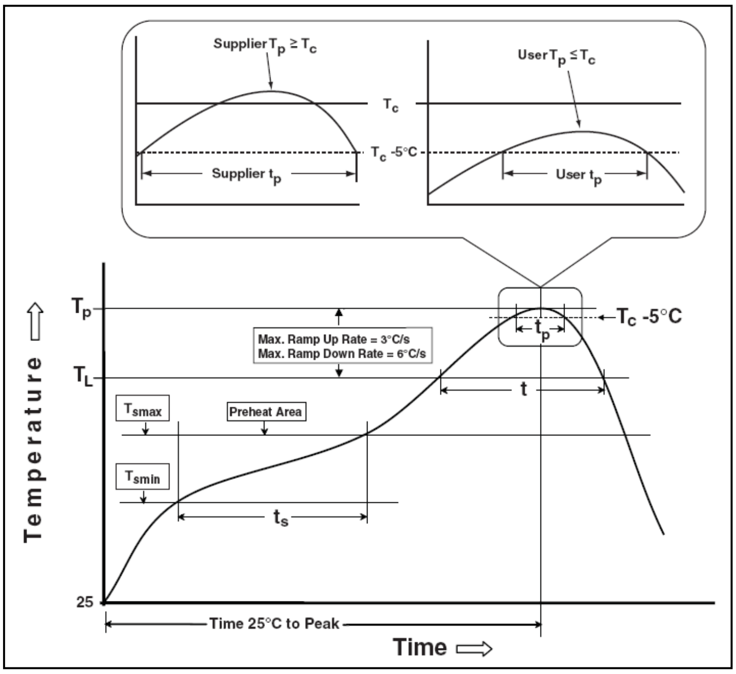
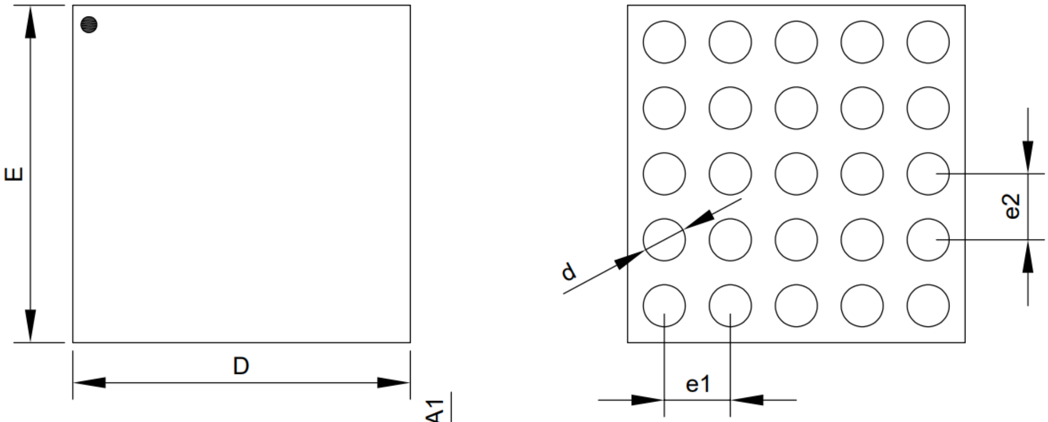
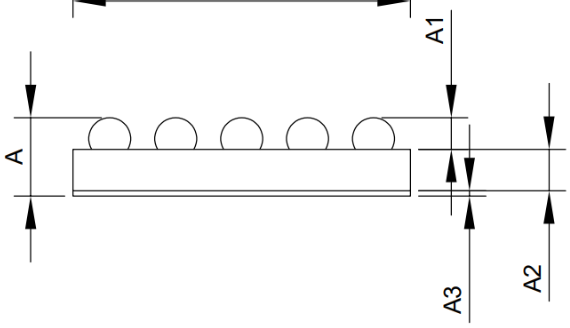


Figure 18. Classification Profile

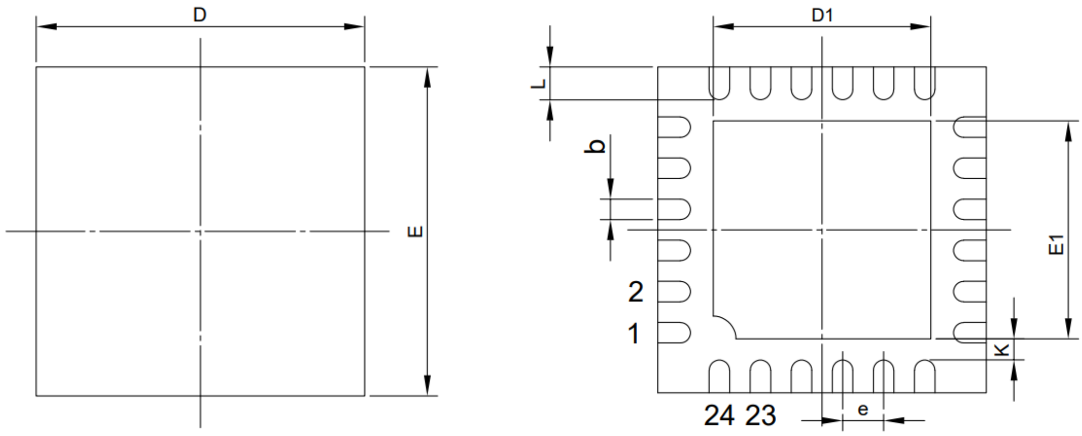
PACKAGE INFORMATION

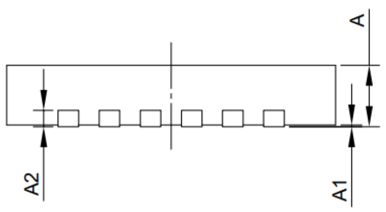




symbol	NOM	TOLER
A	0.595	±0.038
A1	0.24	±0.02
A2	0.315	±0.013
A3	0.04	±0.005
D	2.56	±0.025
E	2.56	±0.025
d	0.32	±0.02
e1	0.5	-
e2	0.5	-

Figure 19. 25 ball, 2.5mm x 2.5mm WLCSP Outline Dimensions





Dimension	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.2	-
D	-	4	-
E	-	4	-
D1	2.5	2.65	2.8
E1	2.5	2.65	2.8
b	0.18	0.25	0.3
K	0.2	-	-
L	0.3	0.4	0.5
ND	6		
NE	6		
e	-	0.5	-
Unit : mm			

Figure 20. 24 Lead, 4mm x 4mm QFN Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 0.5 datasheet, 2019-09-03	
Whole document	New company logo released
Page 1	Remove “Rev0.4 May 2019”
Rev 1.0 datasheet, 2023-07-10	
Whole document	Update the format
Rev 1.1 datasheet, 2024-08-27	
Page 5	Update Ordering Information WLCSP package quantity from 500 to 3000/Reel